



PJC7412

30V N-Channel Enhancement Mode MOSFET – ESD Protected

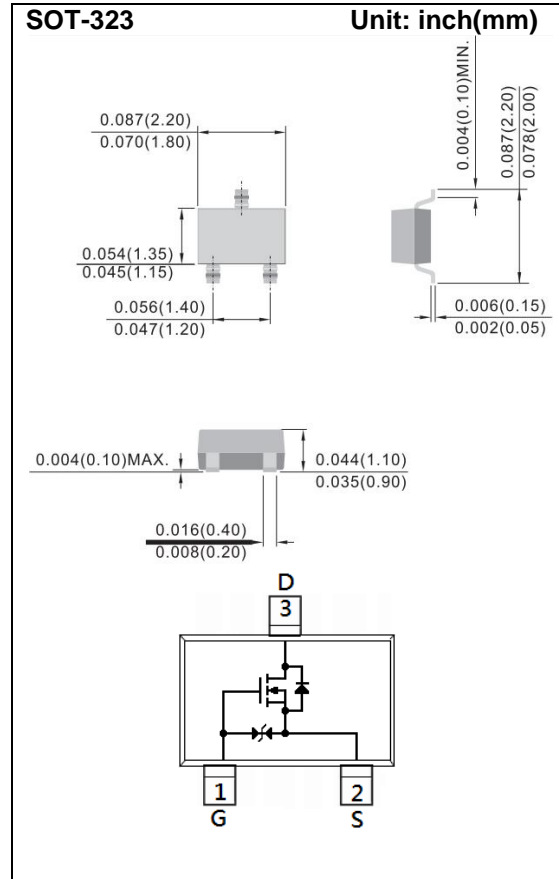
Voltage 30 V **Current** 500mA

Features

- $R_{DS(ON)}$, $V_{GS}@4.5V$, $I_D@500mA < 1.2\Omega$
- $R_{DS(ON)}$, $V_{GS}@2.5V$, $I_D@200mA < 1.6\Omega$
- $R_{DS(ON)}$, $V_{GS}@1.8V$, $I_D@100mA < 2.3\Omega$
- $R_{DS(ON)}$, $V_{GS}@1.5V$, $I_D@10mA < 2.3\Omega$ (typ.)
- Advanced Trench Process Technology
- ESD Protected 2KV HBM
- Specially Designed for Relay driver, Speed line drive, etc.
- Lead free in compliance with EU RoHS 2011/65/EU directive.
- Green molding compound as per IEC61249 Std. (Halogen Free)

Mechanical Data

- Case : SOT-323 Package
- Terminals : Solderable per MIL-STD-750, Method 2026
- Approx. Weight : 0.00018 ounces, 0.005 grams
- Marking : C12



Maximum Ratings and Thermal Characteristics (T_A=25°C unless otherwise noted)

PARAMETER	SYMBOL	LIMIT	UNITS	
Drain-Source Voltage	V _{DS}	30	V	
Gate-Source Voltage	V _{GS}	±10	V	
Continuous Drain Current	I _D	500	mA	
Pulsed Drain Current ^(Note 4)	I _{DM}	1500	mA	
Power Dissipation	P _D	T _A =25°C	350	mW
		Derate above 25°C	2.8	mW/°C
Operating Junction and Storage Temperature Range	T _J , T _{STG}	-55~150	°C	
Typical Thermal Resistance	R _{θJA}	357	°C/W	
- Junction to Ambient ^(Note 3)				



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Electrical Characteristics (T_A=25°C unless otherwise noted)

PARAMETER	SYMBOL	TEST CONDITION	MIN.	TYP.	MAX.	UNITS
Static						
Drain-Source Breakdown Voltage	BV _{DSS}	V _{GS} =0V, I _D =250uA	30	-	-	V
Gate Threshold Voltage	V _{GS(th)}	V _{DS} =V _{GS} , I _D =250uA	0.6	0.85	1.1	V
Drain-Source On-State Resistance	R _{DS(on)}	V _{GS} =4.5V, I _D =500mA	-	0.87	1.2	Ω
		V _{GS} =2.5V, I _D =200mA	-	1.25	1.6	
		V _{GS} =1.8V, I _D =100mA	-	1.6	2.3	
		V _{GS} =1.5V, I _D =10mA	-	2.3	-	
Zero Gate Voltage Drain Current	I _{DSS}	V _{DS} =30V, V _{GS} =0V	-	0.01	1	uA
Gate-Source Leakage Current	I _{GSS}	V _{GS} =±8V, V _{DS} =0V	-	-	±10	
		V _{GS} =±5V, V _{DS} =0V	-	-	±1	
Dynamic (Note 5)						
Total Gate Charge	Q _g	V _{DS} =15V, I _D =500mA, V _{GS} =4.5V (Note 1,2)	-	0.87	-	nC
Gate-Source Charge	Q _{gs}		-	0.26	-	
Gate-Drain Charge	Q _{gd}		-	0.16	-	
Input Capacitance	C _{iss}	V _{DS} =15V, V _{GS} =0V, f=1.0MHZ	-	34	-	pF
Output Capacitance	C _{oss}		-	8.9	-	
Reverse Transfer Capacitance	C _{rss}		-	2.5	-	
Turn-On Delay Time	t _{d(on)}		V _{DD} =15V, I _D =80mA, V _{GS} =4.0V, R _G =6Ω (Note 1,2)	-	7.1	
Turn-On Rise Time	t _r	-		20	-	
Turn-Off Delay Time	t _{d(off)}	-		41	-	
Turn-Off Fall Time	t _f	-		31	-	
Drain-Source Diode						
Maximum Continuous Drain-Source Diode Forward Current	I _s	---	-	-	500	mA
Diode Forward Voltage	V _{SD}	I _s =500mA, V _{GS} =0V	-	0.88	1.3	V

NOTES :

1. Pulse width ≤ 300us, Duty cycle ≤ 2%
2. Essentially independent of operating temperature typical characteristics.
3. R_{θJA} is the sum of the junction-to-case and case-to-ambient thermal resistance where the case thermal reference is defined as the solder mounting surface of the drain pins mounted on a 1 inch FR-4 with 2oz. square pad of copper.
4. The maximum current rating is package limited.
5. Guaranteed by design, not subject to production testing.



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TYPICAL CHARACTERISTIC CURVES

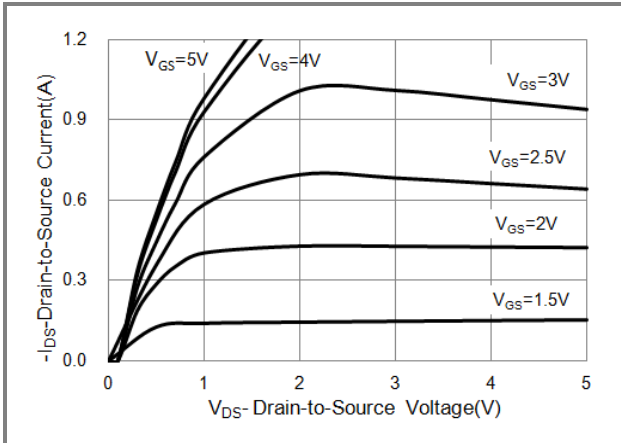


Fig.1 On-Region Characteristics

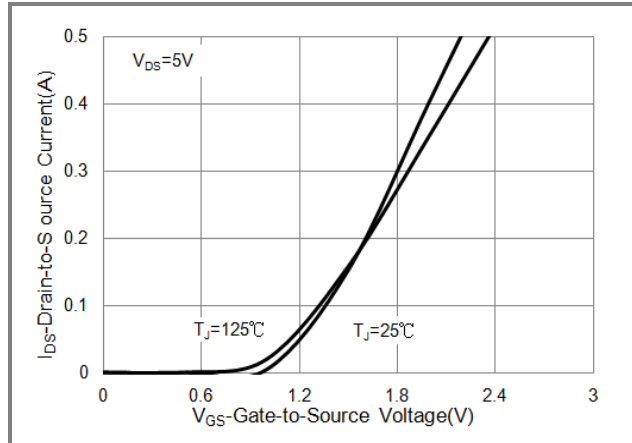


Fig.2 Transfer Characteristics

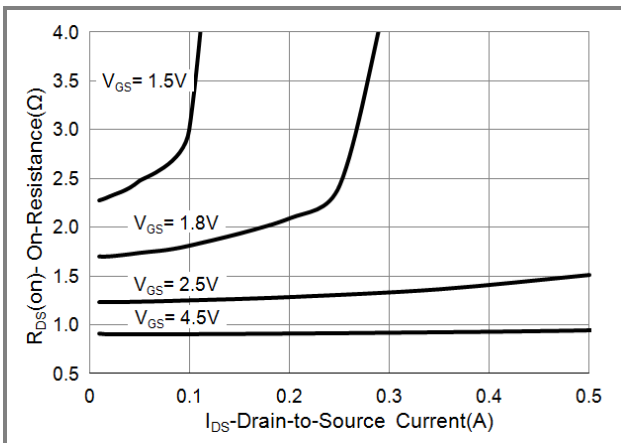


Fig.3 On-Resistance vs. Drain Current

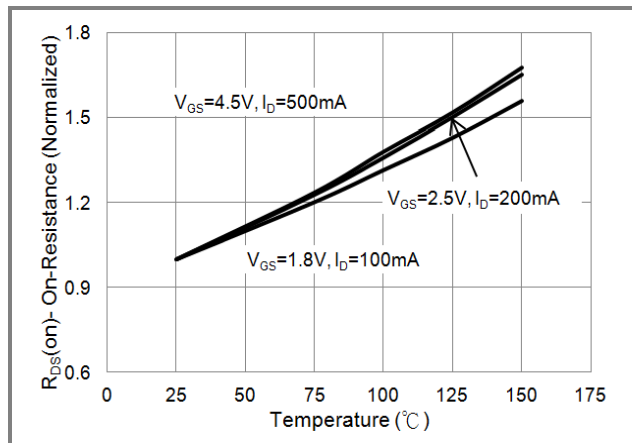


Fig.4 On-Resistance vs. Junction temperature

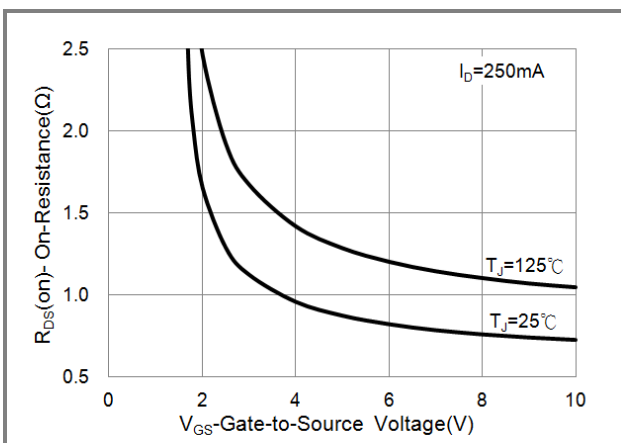


Fig.5 On-Resistance Variation with V_GS.

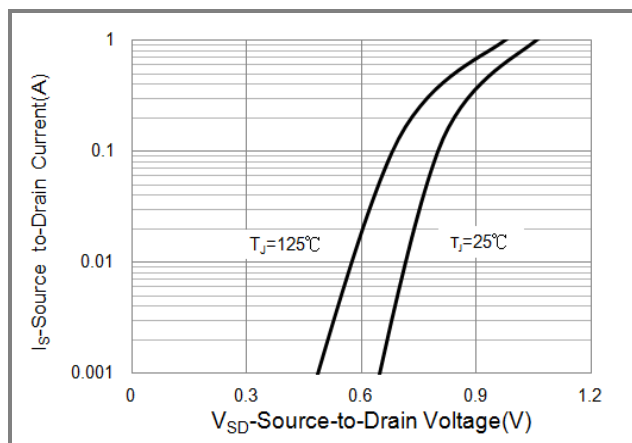


Fig.6 Body Diode Characteristics



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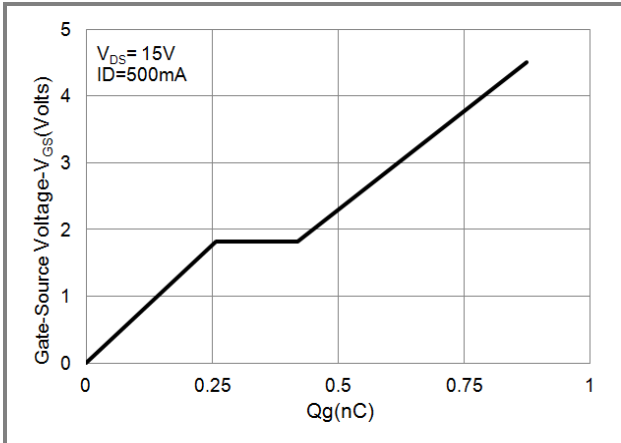


Fig.7 Gate-Charge Characteristics

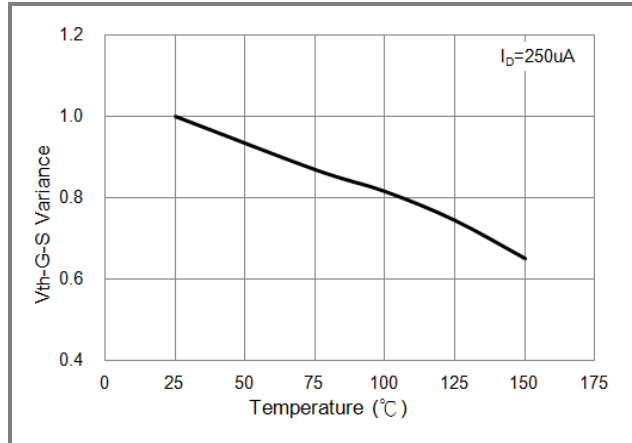


Fig.8 Threshold Voltage Variation with Temperature.

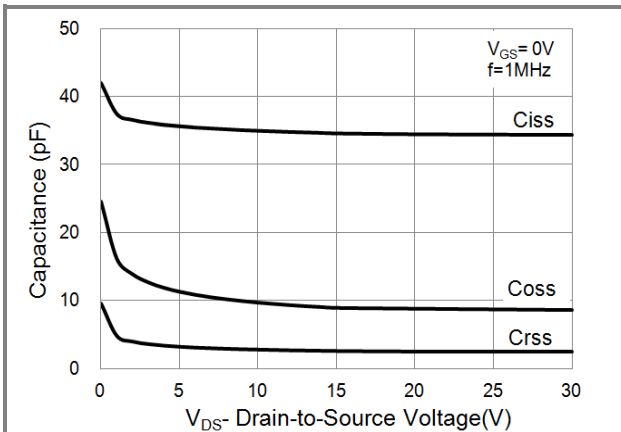


Fig.9 Capacitance vs. Drain-Source Voltage.

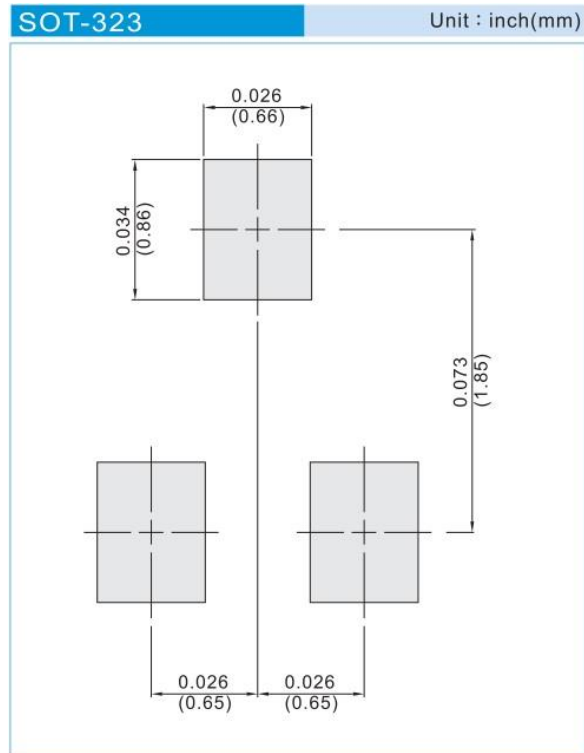


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PART NO. PACKING CODE VERSION

Part No. Packing Code	Package Type	Packing Type	Marking	Version
PJC7412_R1_00001	SOT-323	3K pcs / 7" reel	C12	Halogen free
PJC7412_R2_00001	SOT-323	12K pcs / 13" reel	C12	Halogen free

MOUNTING PAD LAYOUT





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