



PJQ1901

20V P-Channel Enhancement Mode MOSFET

Voltage **-20 V** **Current** **-0.75 A**

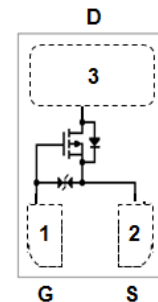
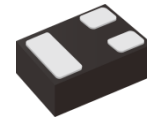
Features

- Low Voltage Drive (1.2V)
- Advanced Trench Process Technology
- ESD Protected
- Specially Designed for Switch Load, PWM Application, etc
- Lead free in compliance with EU RoHS 2.0
- Green molding compound as per IEC 61249 standard

Mechanical Data

- Case : DFN1006-3L Package
- Terminals : Solderable per MIL-STD-750, Method 2026
- Approx. Weight : 0.00002 ounces, 0.0007 grams

DFN1006-3L



Maximum Ratings and Thermal Characteristics (T_A=25°C unless otherwise noted)

PARAMETER	SYMBOL	LIMIT	UNITS	
Drain-Source Voltage	V _{DS}	-20	V	
Gate-Source Voltage	V _{GS}	±10		
Continuous Drain Current ^(Note 4)	I _D	-0.75	A	
Pulsed Drain Current ^(Note 1)	I _{DM}	-2		
Power Dissipation	P _D	T _A =25°C	900	mW
		Derate above 25°C	7.2	mW/°C
Operating Junction and Storage Temperature Range	T _J , T _{STG}	-55~150	°C	
Typical Thermal Resistance	R _{θJA}	139	°C/W	
- Junction to Ambient, t<10s ^(Note 5)				



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Electrical Characteristics (T_A=25°C unless otherwise noted)

PARAMETER	SYMBOL	TEST CONDITION	MIN.	TYP.	MAX.	UNITS
Static						
Drain-Source Breakdown Voltage	BV _{DSS}	V _{GS} =0V, I _D =-250uA	-20	-	-	V
Gate Threshold Voltage	V _{GS(th)}	V _{DS} =V _{GS} , I _D =-250uA	-0.3	-0.59	-1.0	
Drain-Source On-State Resistance	R _{DSON}	V _{GS} =-4.5V, I _D =-400mA	-	0.85	1.2	Ω
		V _{GS} =-2.5V, I _D =-150mA	-	0.98	1.5	
		V _{GS} =-1.8V, I _D =-80mA	-	1.15	2.2	
		V _{GS} =-1.5V, I _D =-30mA	-	1.33	3.6	
		V _{GS} =-1.2V, I _D =-10mA	-	1.5	6.0	
Zero Gate Voltage Drain Current	I _{DSS}	V _{DS} =-16V, V _{GS} =0V	-	-	-1	uA
Gate-Source Leakage Current	I _{GSS}	V _{GS} =±8V, V _{DS} =0V	-	-	±10	
Dynamic ^(Note 6)						
Total Gate Charge	Q _g	V _{DS} =-10V, I _D =-200mA, V _{GS} =-4.5V ^(Note 2)	-	1.4	-	nC
Gate-Source Charge	Q _{gs}		-	0.19	-	
Gate-Drain Charge	Q _{gd}		-	0.2	-	
Input Capacitance	C _{iss}	V _{DS} =-10V, V _{GS} =0V, f=1.0MHZ	-	38	-	pF
Output Capacitance	C _{oss}		-	15	-	
Reverse Transfer Capacitance	C _{rss}		-	9	-	
Turn-On Delay Time	t _{d(on)}	V _{DD} =-10V, I _D =-150mA, V _{GS} =-4.5V, R _G =6Ω ^(Note 1,2)	-	7.2	-	ns
Turn-On Rise Time	t _r		-	21	-	
Turn-Off Delay Time	t _{d(off)}		-	85	-	
Turn-Off Fall Time	t _f		-	116	-	
Drain-Source Diode						
Diode Forward Current	I _S	---	-	-	-200	mA
Diode Forward Voltage	V _{SD}	I _S =-200mA, V _{GS} =0V	-	-0.93	-1.3	V

Notes :

- 1.Pulse width<300us, Duty cycle<2%.
- 2.Essentially independent of operating temperature typical characteristics.
- 3.Repetitive rating, pulse width limited by junction temperature T_J(MAX)=150°C.Ratings are based on low frequency and duty cycles to keep initial T_J =25°C.
- 4.The maximum current rating is package limited.
- 5.R_{θJA} is the sum of the junction-to-case and case-to-ambient thermal resistance where the case thermal reference is defined as the solder mounting surface of the drain pins. Mounted on a 1 inch² with 2oz.square pad of copper.
- 6.Guaranteed by design, not subject to production testing.



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TYPICAL CHARACTERISTIC CURVES

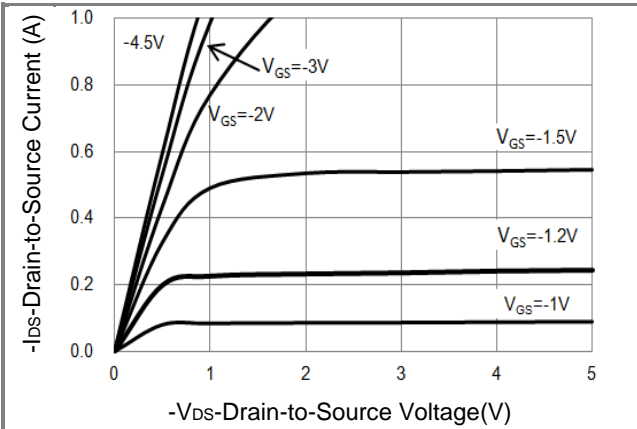


Fig.1 Output Characteristics

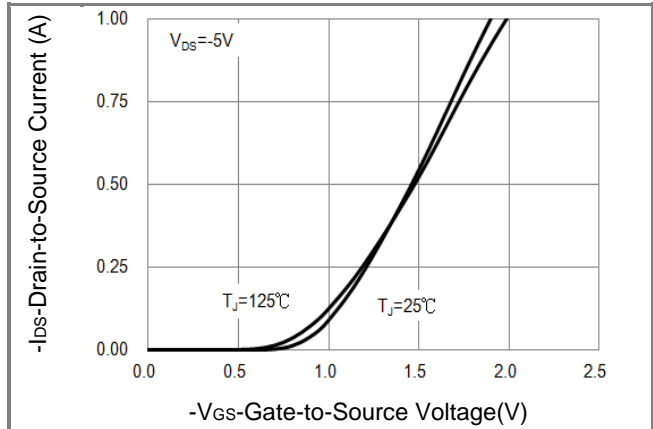


Fig.2 Transfer Characteristics

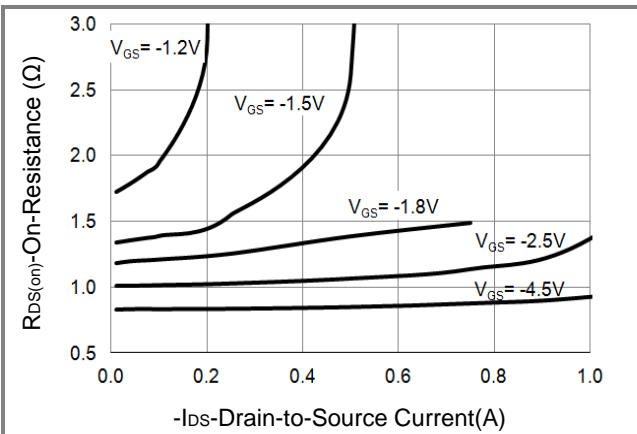


Fig.3 On-Resistance vs. Drain Current

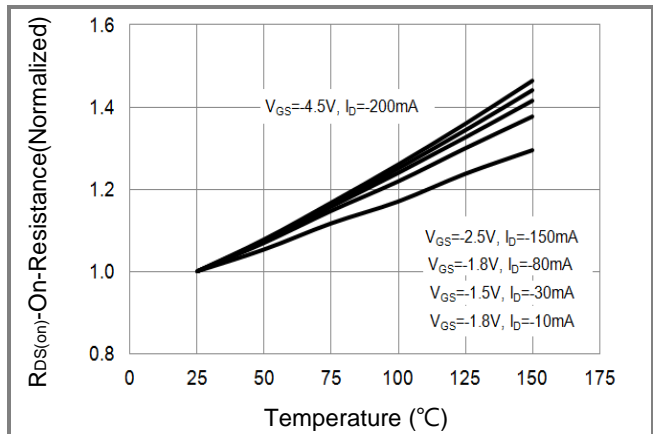


Fig.4 On-Resistance vs. Junction temperature

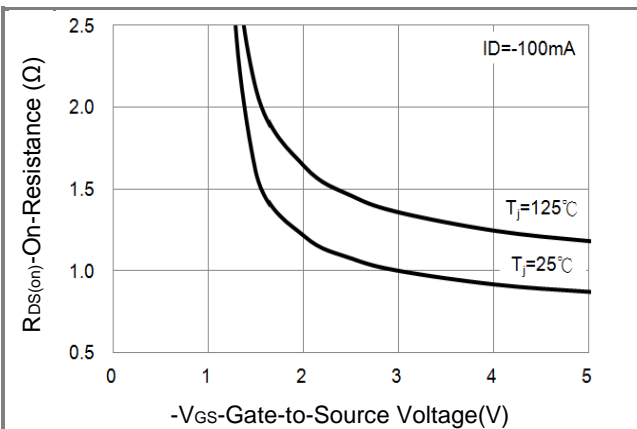


Fig.5 On-Resistance Variation with V_GS

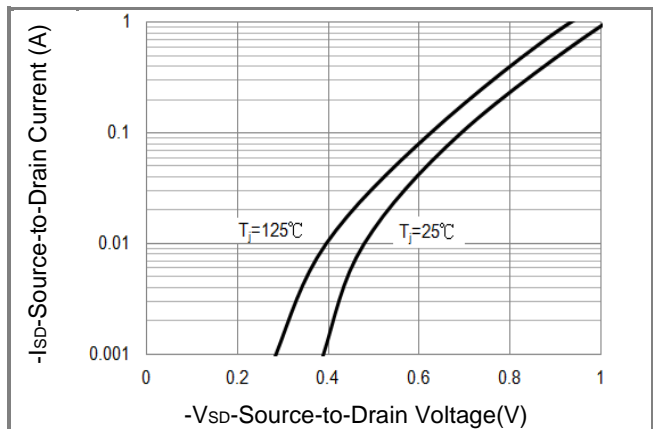


Fig.6 Source-Drain Diode Forward Voltage



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TYPICAL CHARACTERISTIC CURVES

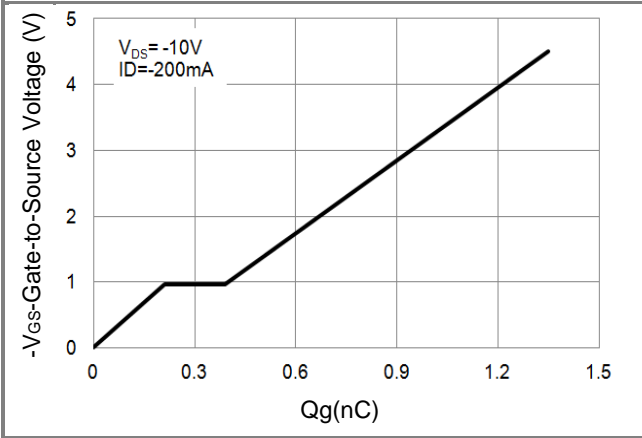


Fig.7 Gate-Charge Characteristics

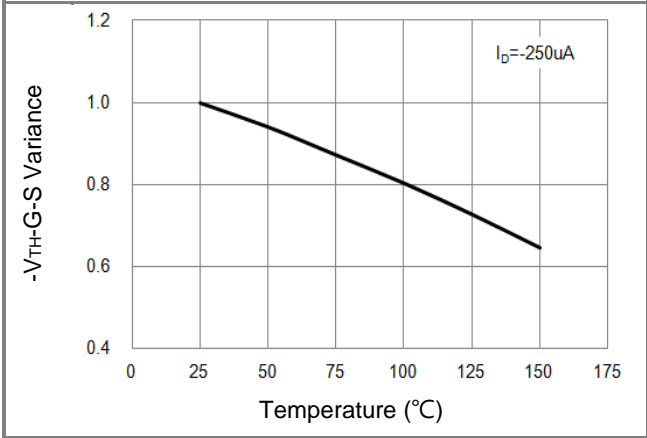


Fig.8 Breakdown Voltage Variation vs. Temperature

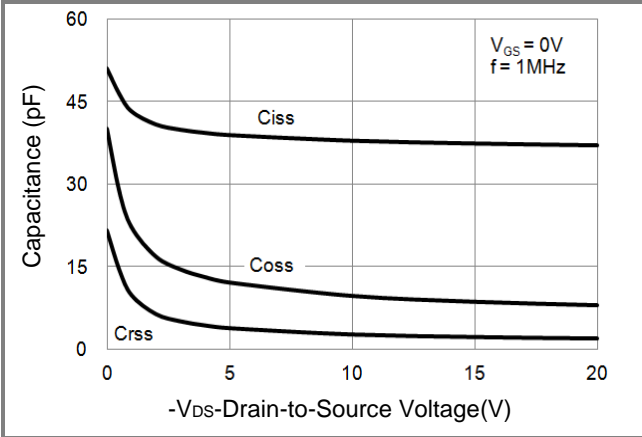


Fig.9 Capacitance vs. Drain-Source Voltage

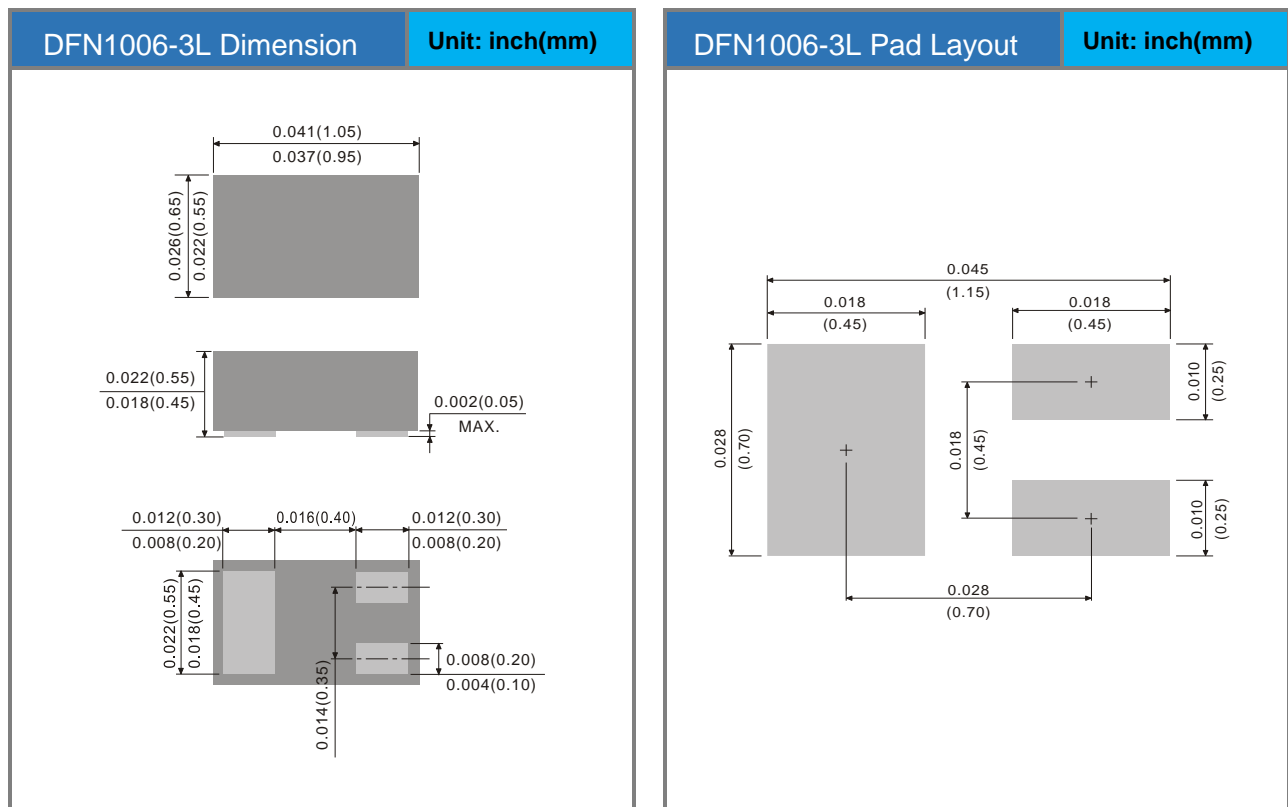


PJQ1901

Part No. Packing Code Version

Part No. Packing Code	Package Type	Packing Type	Marking	Version
PJQ1901_R1_00201	DFN1006-3L	10K pcs / 7" reel	1	Halogen free RoHS compliant

Packaging Information & Mounting Pad Layout





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