



# PJQ5474A

## 100V N-Channel Enhancement Mode MOSFET

<b>Voltage</b>	<b>100 V</b>	<b>Current</b>	<b>18A</b>
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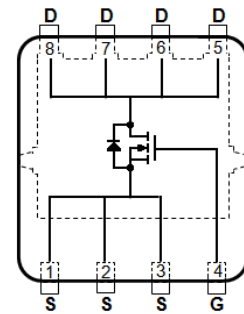
### Features

- $R_{DS(ON)}$ ,  $V_{GS}@10V$ ,  $I_D@18A < 50m\Omega$
- $R_{DS(ON)}$ ,  $V_{GS}@4.5V$ ,  $I_D@15A < 55m\Omega$
- Advanced Trench Process Technology
- High density cell design for ultra low on-resistance
- Lead free in compliance with EU RoHS 2.0
- Green molding compound as per IEC 61249 standard

### Mechanical Data

- Case: DFN5060-8L Package
- Terminals: Solderable per MIL-STD-750, Method 2026
- Approx. Weight: 0.0028 ounces, 0.08 grams
- Marking: Q5474A

DFN5060-8L



## Maximum Ratings and Thermal Characteristics ( $T_A=25^\circ C$ unless otherwise noted)

PARAMETER	SYMBOL	LIMIT	UNITS	
Drain-Source Voltage	$V_{DS}$	100	V	
Gate-Source Voltage	$V_{GS}$	$\pm 20$	V	
Continuous Drain Current	$I_D$	18	A	
Pulsed Drain Current	$I_{DM}$	36	A	
Single Pulse Avalanche Energy <sup>(Note 5)</sup>	$E_{AS}$	16.2	mJ	
Power Dissipation	$P_D$	$T_C=25^\circ C$	52	W
		Derate above $25^\circ C$	416	mW/ $^\circ C$
Operating Junction and Storage Temperature Range	$T_J, T_{STG}$	-55~150	$^\circ C$	
Typical Thermal resistance	$R_{\theta JC}$	2.4	$^\circ C/W$	
- Junction to Ambient, $t < 10s$ <sup>(Note 3)</sup>				



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## Electrical Characteristics (T<sub>A</sub>=25°C unless otherwise noted)

PARAMETER	SYMBOL	TEST CONDITION	MIN.	TYP.	MAX.	UNITS
<b>Static</b>						
Drain-Source Breakdown Voltage	BV <sub>DSS</sub>	V <sub>GS</sub> =0V, I <sub>D</sub> =250uA	100	-	-	V
Gate Threshold Voltage	V <sub>GS(th)</sub>	V <sub>DS</sub> =V <sub>GS</sub> , I <sub>D</sub> =250uA	1.0	1.5	2.5	V
Drain-Source On-State Resistance	R <sub>DS(on)</sub>	V <sub>GS</sub> =10V, I <sub>D</sub> =18A	-	37	50	mΩ
		V <sub>GS</sub> =4.5V, I <sub>D</sub> =15A	-	38	55	
Zero Gate Voltage Drain Current	I <sub>DSS</sub>	V <sub>DS</sub> =80V, V <sub>GS</sub> =0V	-	0.03	1.0	uA
Gate-Source Leakage Current	I <sub>GSS</sub>	V <sub>GS</sub> =±20V, V <sub>DS</sub> =0V	-	±10	±100	nA
<b>Dynamic</b> (Note 7)						
Total Gate Charge	Q <sub>g</sub>	V <sub>DS</sub> =80V, I <sub>D</sub> =18A, V <sub>GS</sub> =10V (Note 1,2)	-	61	-	nC
Gate-Source Charge	Q <sub>gs</sub>		-	8.8	-	
Gate-Drain Charge	Q <sub>gd</sub>		-	11	-	
Input Capacitance	C <sub>iss</sub>	V <sub>DS</sub> =15V, V <sub>GS</sub> =0V, f=1.0MHZ	-	3555	-	pF
Output Capacitance	C <sub>oss</sub>		-	119	-	
Reverse Transfer Capacitance	C <sub>rss</sub>		-	56	-	
Turn-On Delay Time	t <sub>d(on)</sub>	V <sub>DD</sub> =50V, I <sub>D</sub> =18A, V <sub>GS</sub> =10V, R <sub>G</sub> =3.3Ω (Note 1,2)	-	16	-	ns
Turn-On Rise Time	t <sub>r</sub>		-	50	-	
Turn-Off Delay Time	t <sub>d(off)</sub>		-	64	-	
Turn-Off Fall Time	t <sub>f</sub>		-	18	-	
<b>Drain-Source Diode</b>						
Maximum Continuous Drain-Source Diode Forward Current	I <sub>S</sub>	---	-	-	18	A
Diode Forward Voltage	V <sub>SD</sub>	I <sub>S</sub> =1.0A, V <sub>GS</sub> =0V	-	0.7	1.2	V

**NOTES :**

1. Pulse width ≤ 300us, Duty cycle ≤ 2%
2. Essentially independent of operating temperature typical characteristics.
3. The maximum current rating is package limited.
4. Repetitive rating, pulse width limited by junction temperature T<sub>J</sub>(MAX)=150°C. Ratings are based on low frequency and duty cycles to keep initial T<sub>J</sub> = 25°C.
5. The test condition is L=0.1mH, I<sub>AS</sub>=18A, V<sub>DD</sub>=25V, V<sub>GS</sub>=10V
6. R<sub>θJA</sub> is the sum of the junction-to-case and case-to-ambient thermal resistance where the case thermal reference is defined as the solder mounting surface of the drain pins. Mounted on a 1 inch<sup>2</sup> with 2oz.square pad of copper.
7. Guaranteed by design, not subject to production testing.



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## TYPICAL CHARACTERISTIC CURVES

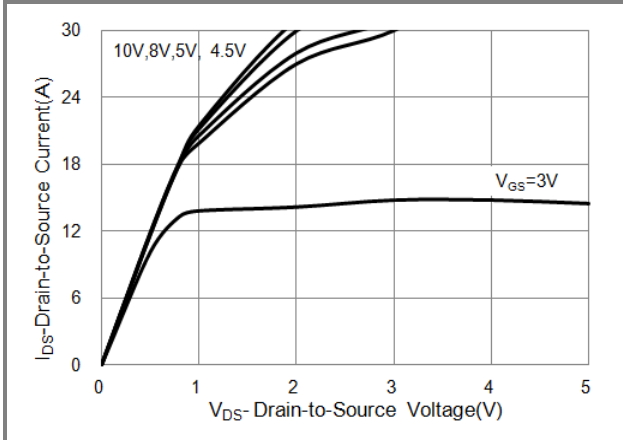


Fig.1 On-Region Characteristics

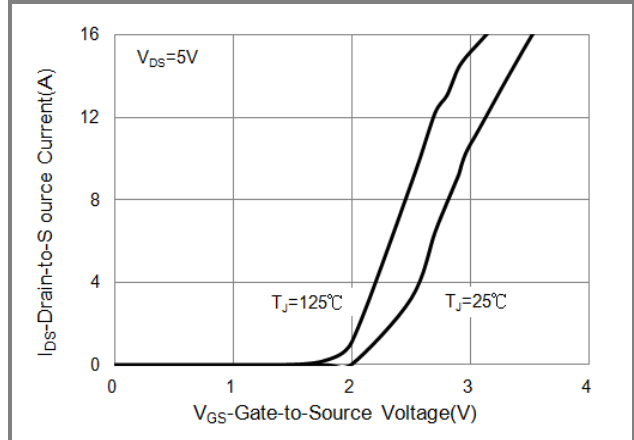


Fig.2 Transfer Characteristics

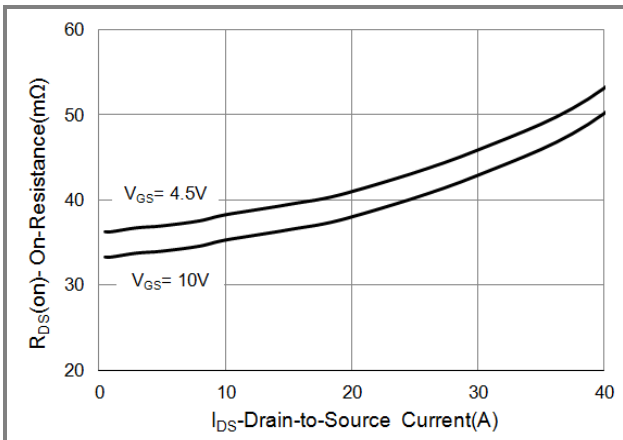


Fig.3 On-Resistance vs. Drain Current

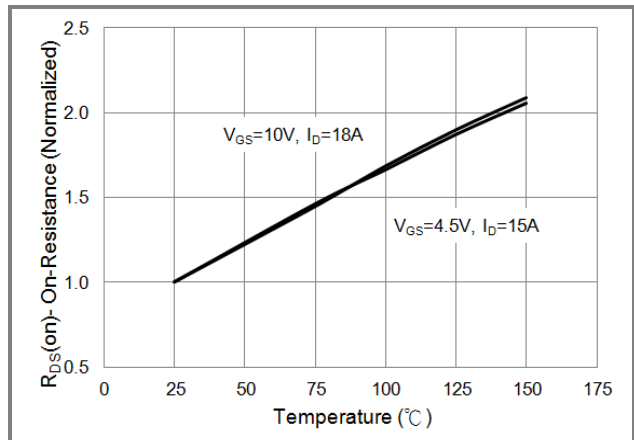


Fig.4 On-Resistance vs. Junction temperature

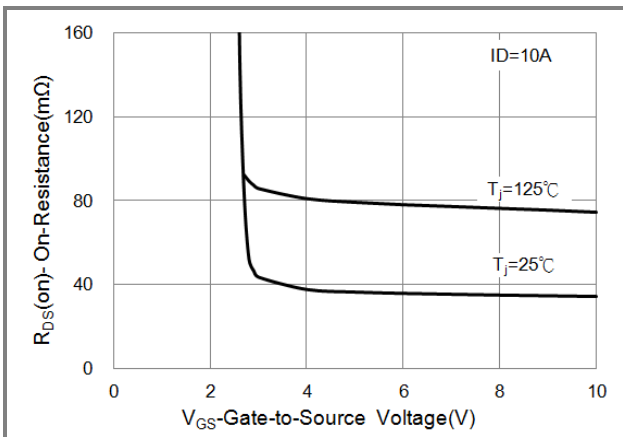


Fig.5 On-Resistance Variation with VGS.

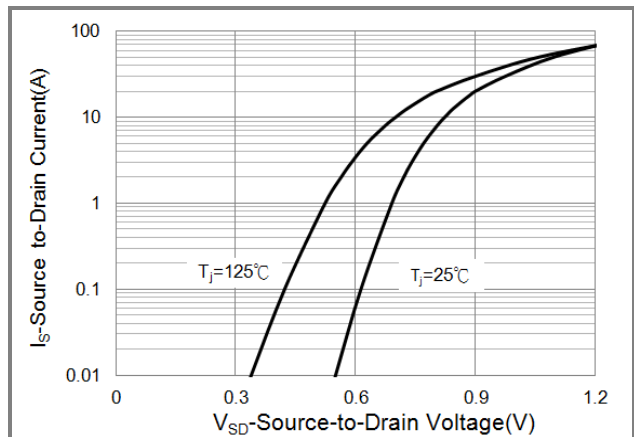


Fig.6 Body Diode Characteristics



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## TYPICAL CHARACTERISTIC CURVES

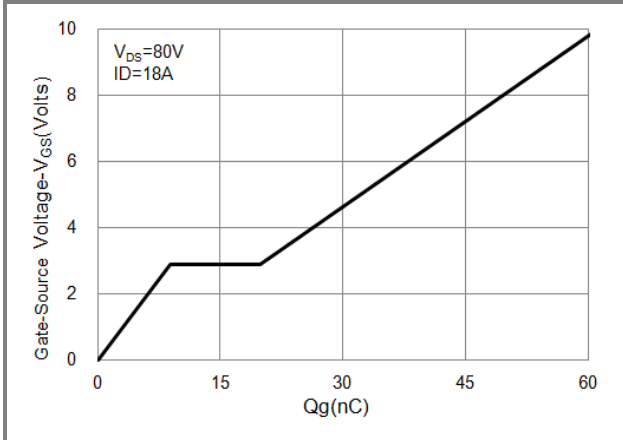


Fig.7 Gate-Charge Characteristics

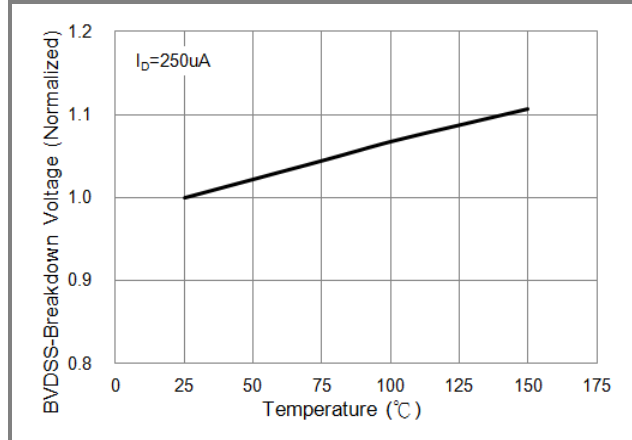


Fig.8 Breakdown Voltage Variation vs. Temperature

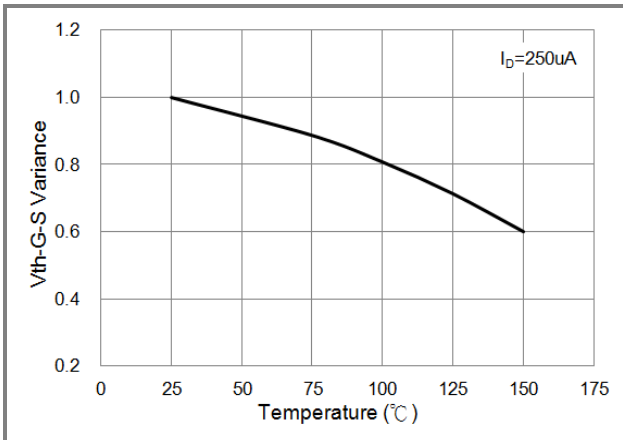


Fig.9 Threshold Voltage Variation with Temperature.

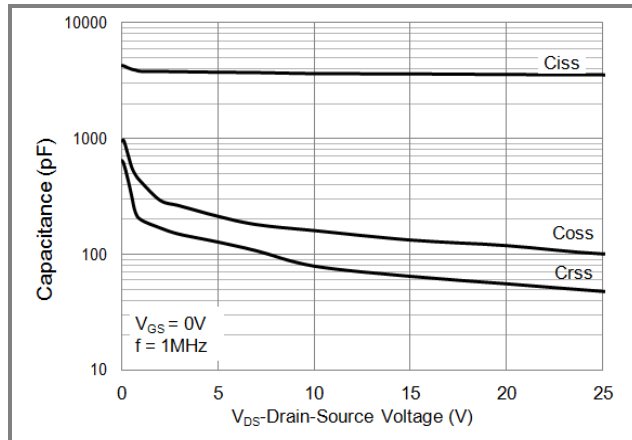


Fig.10 Capacitance vs. Drain-Source Voltage.

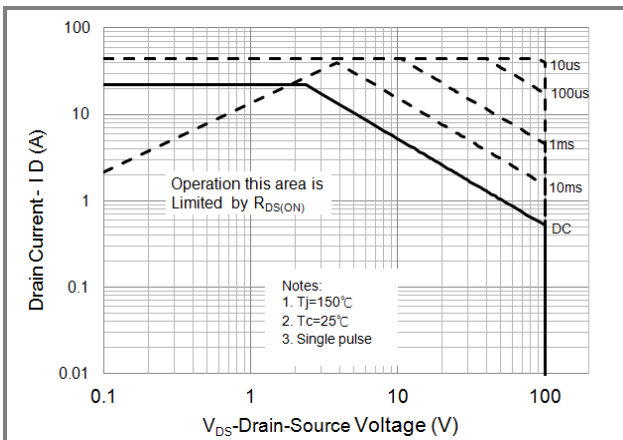


Fig.11 Maximum Safe Operating Area



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## TYPICAL CHARACTERISTIC CURVES

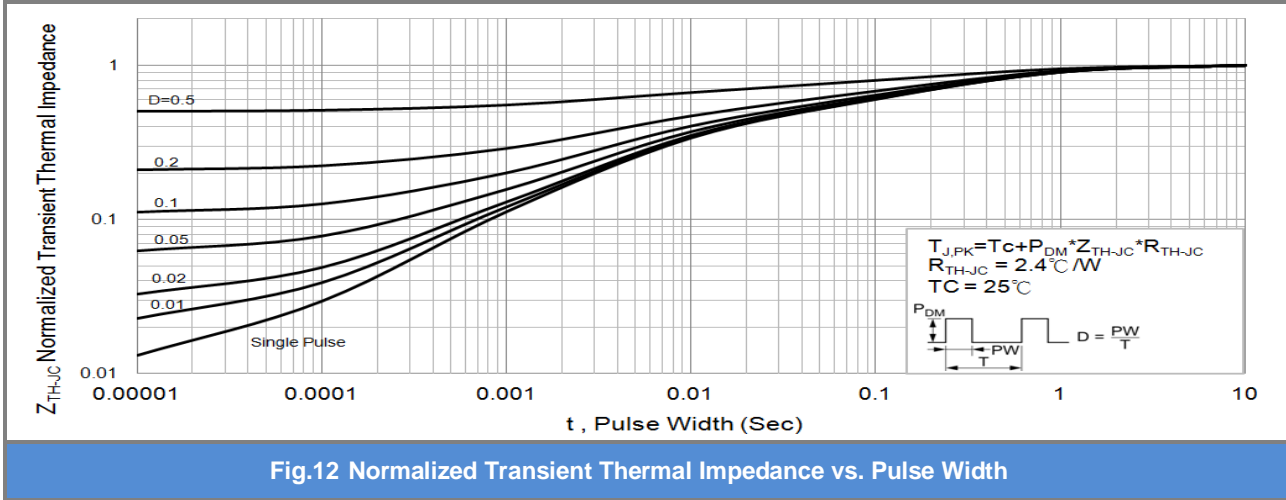


Fig.12 Normalized Transient Thermal Impedance vs. Pulse Width

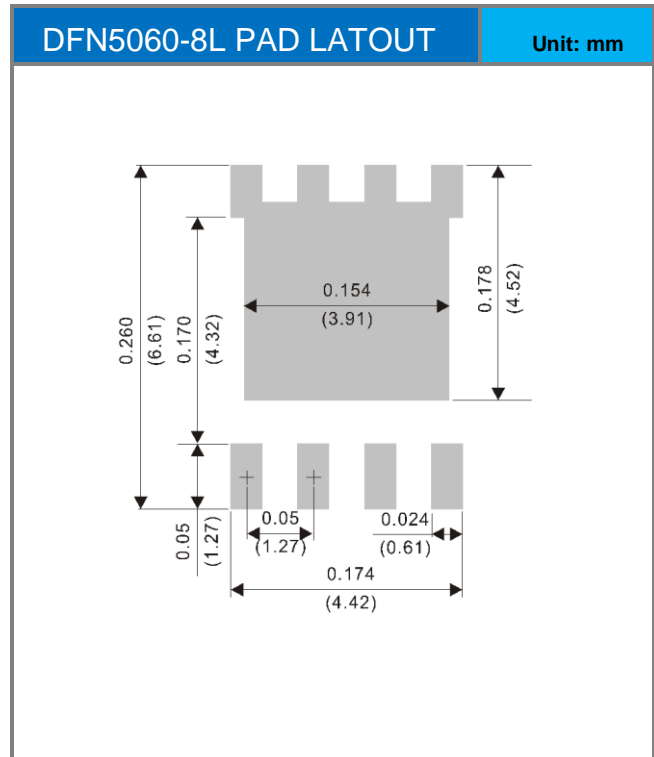
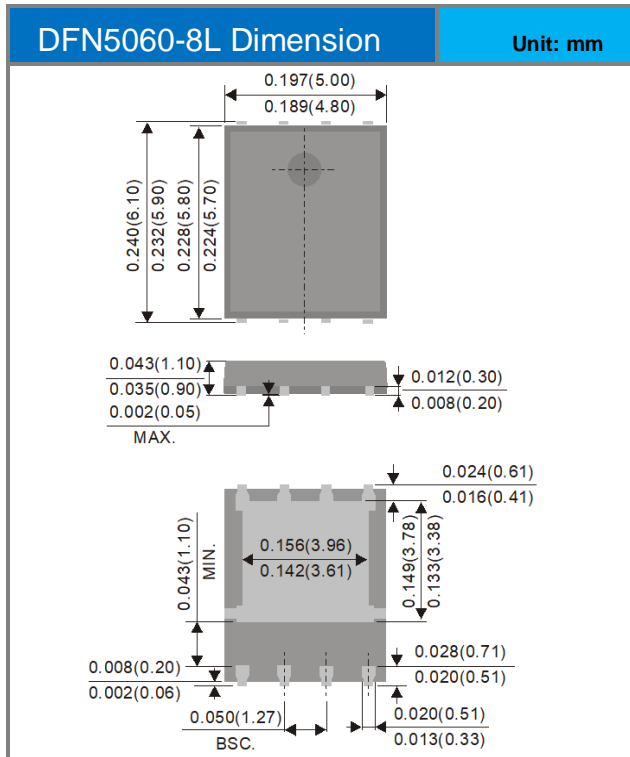


# PJQ5474A

## PART NO PACKING CODE VERSION

Part No Packing Code	Package Type	Packing type	Marking	Version
PJQ5474A_R2_00001	DFN5060-8L	3000pcs / 13" reel	Q5474A	Halogen free

## Packaging Information & Mounting Pad Layout





## PJQ5474A

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