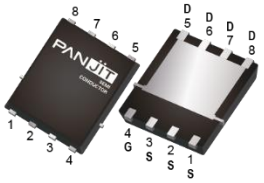
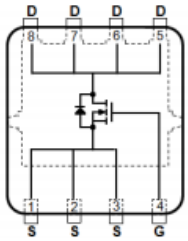
100V N-Channel Enhancement Mode MOSFET

Voltage	**100 V**	**$R_{DS(on),max}$**	**3.9 mΩ**
Current	**126 A**	**$Q_{G\ (TYP)}$**	**46 nC**

DFN5060X-8L





Top side view

Feature

- $R_{DS(ON),max}$ < 3.9 mΩ at V_{GS} = 10 V, I_D = 60 A
- $R_{DS(ON),max}$ < 5.9 mΩ at V_{GS} = 6 V, I_D = 30 A
- High switching speed
- Low reverse transfer capacitance
- Lead free in compliance with EU RoHS 2.0
- Green molding compound as per IEC 61249 standard

Mechanical Data

- Case: DFN5060X-8L Package
- Terminals: Solderable per MIL-STD-750, Method 2026
- Approx. Weight: 0.087 grams

Application

- SR solutions of PD Charger, Brick Power, 48V DC/DC converter

Absolute Maximum Ratings (T_A = 25 °C unless otherwise specified)

PARAMETER		SYMBOL	LIMIT	UNITS
Drain-Source Voltage		V_{DS}	100	V
Gate-Source Voltage		V_{GS}	±20	
Continuous Drain Current (Note 3)	T_C=25 °C	I_D	126	A
	T_C=100 °C		89	
Pulsed Drain Current (Note 6)	T_C=25 °C	I_{DM}	504	A
Single Pulse Avalanche Current (Note 5)		I_{AS}	54	A
Single Pulse Avalanche Energy (Note 5)		E_{AS}	145	mJ
Power Dissipation	T_C=25 °C	P_D	125	W
	T_C=100 °C		62.5	
Operating Junction and Storage Temperature Range		T_J,T_{STG}	-55~175	°C

Thermal Characteristics

PARAMETER		SYMBOL	VALUES			UNITS
			MIN.	TYP.	MAX.	
Thermal Resistance	Junction-to-Case (Bottom)	$R_{\theta JC}$	-	0.8	1.2	°C/W
	Junction-to-Ambient (Note 4)	$R_{\theta JA}$	-	-	50	°C/W

Electrical Characteristics (T_A = 25 °C unless otherwise specified)

PARAMETER	SYMBOL	TEST CONDITION	MIN.	TYP.	MAX.	UNITS
Static Characteristics						
Drain-Source Breakdown Voltage	BV_{DSS}	V_{GS}=0 V, I_D=250 μA	100	-	-	V
Gate Threshold Voltage	$V_{GS(th)}$	V_{DS}=V_{GS}, I_D=300 μA	1.8	2.8	3.8	
Drain-Source On-State Resistance (Note 1)	$R_{DS(on)}$	V_{GS}=10 V, I_D=60 A	-	3.5	3.9	mΩ
		V_{GS}=6 V, I_D=30 A	-	4.5	5.9	
Zero Gate Voltage Drain Current	I_{DSS}	V_{DS}=100 V, V_{GS}=0 V	-	-	2	μA
Gate-Source Leakage Current	I_{GSS}	V_{GS}=±20 V, V_{DS}=0 V	-	-	±100	nA
Transfer characteristics (Note 1)	g_{fs}	V_{DS}=10 V, I_D=60 A	-	110	-	S
Dynamic Characteristics (Note 6)						
Total Gate Charge	Q_g	V_{DS}=50 V, I_D=60 A, V_{GS}=10 V	-	46	60	nC
Gate-Source Charge	Q_{gs}		-	16	-	
Gate-Drain Charge	Q_{gd}		-	7.0	-	
Gate Plateau Voltage	$V_{plateau}$		-	4.5	-	V
Input Capacitance	C_{iss}	V_{DS}=50 V, V_{GS}=0 V, f=250 kHz	-	3110	4040	pF
Output Capacitance	C_{oss}		-	1220	1590	
Reverse Transfer Capacitance	C_{rss}		-	19	-	
Output Charge	Q_{oss}	V_{DS}=50 V, V_{GS}=0 V	-	93	121	nC
Turn-On Delay Time	$t_{d(on)}$	V_{DD}=50 V, I_D=60 A, V_{GS}=10 V, R_G=1.8 Ω (Note 2)	-	15.3	-	ns
Rise Time	t_r		-	8.7	-	
Turn-Off Delay Time	$t_{d(off)}$		-	24	-	
Fall Time	t_f		-	5.4	-	
Gate Resistance	R_g	f =1.0 MHz	-	0.4	0.8	Ω
Drain-Source Diode						
Diode Forward Voltage	V_{SD}	I_S=60 A, V_{GS}=0 V	-	0.9	1.2	V
Reverse Recovery Charge	Q_{rr}	I_F=60 A, V_{DD}=50 V, di/dt=100 A/μs	-	180	-	nC
Reverse Recovery Time	T_{rr}		-	89	-	ns

NOTES :

1. Pulse width ≤ 300 μs, Duty cycle ≤ 2 %.
2. Essentially independent of operating temperature typical characteristics.
3. The maximum drain current calculated by maximum junction temperature and thermal impedance. It can be varied by application and environment.
4. $R_{\theta JA}$ is the sum of the junction-to-case and case-to-ambient thermal resistance where the case thermal reference is defined as the solder mounting surface of the drain pins. Mounted on a 1 $inch^2$ with 2oz.square pad of copper.
5. E_{AS} is calculated based on the condition of L = 0.1 mH, I_{AS} = 54 A, V_{DD} = 50 V, V_{GS} = 10 V and 100% test in production.
6. Guaranteed by design, not subject to production testing.

TYPICAL CHARACTERISTIC CURVES

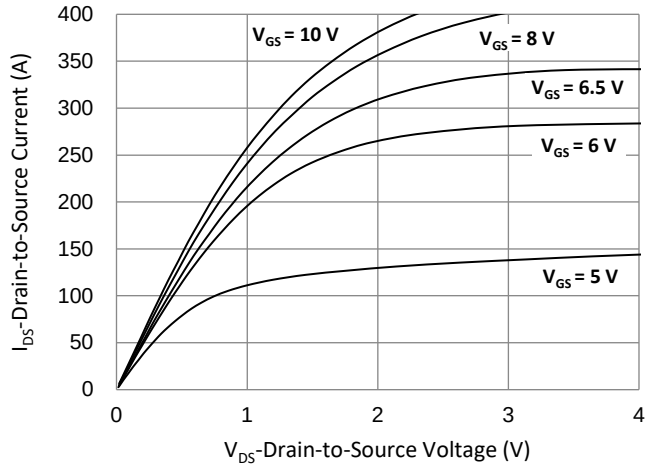


Fig.1 Output Characteristics

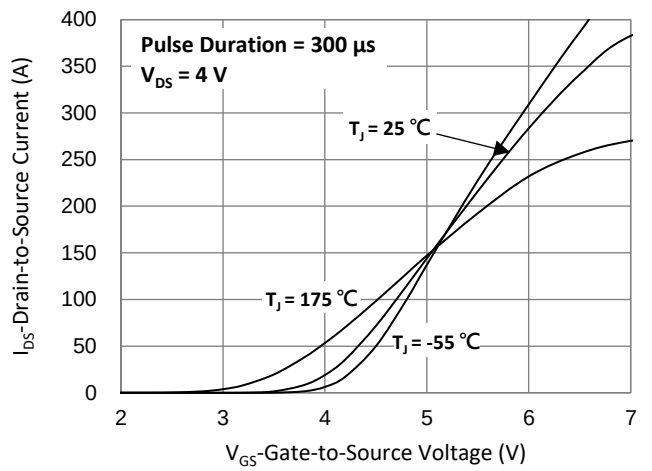


Fig.2 Transfer Characteristics

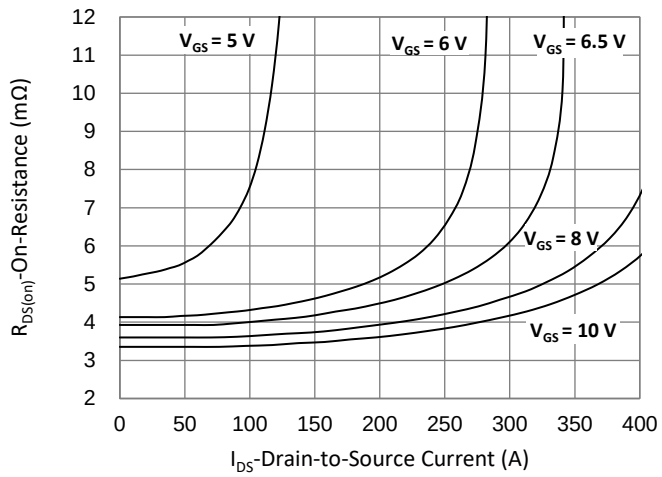


Fig.3 On-Resistance vs. Drain Current

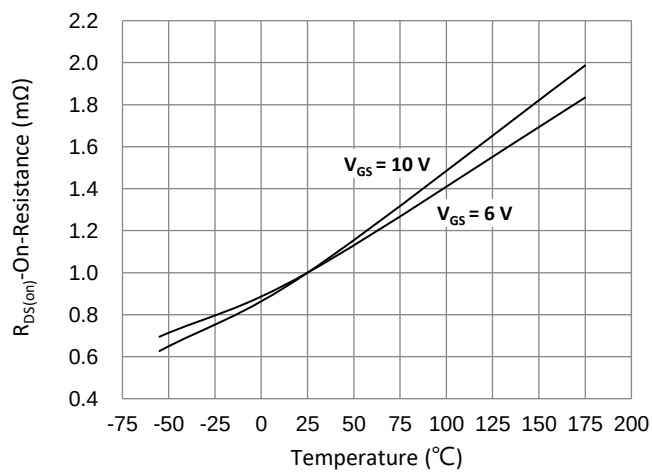


Fig.4 On-Resistance vs. Junction temperature

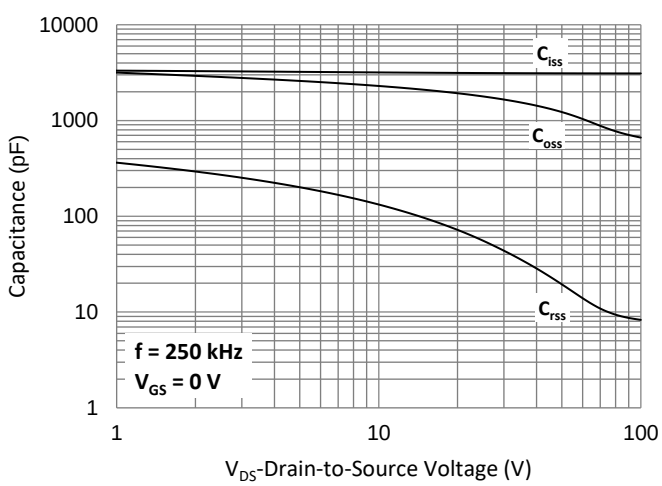


Fig.5 Capacitance vs. Drain-Source Voltage

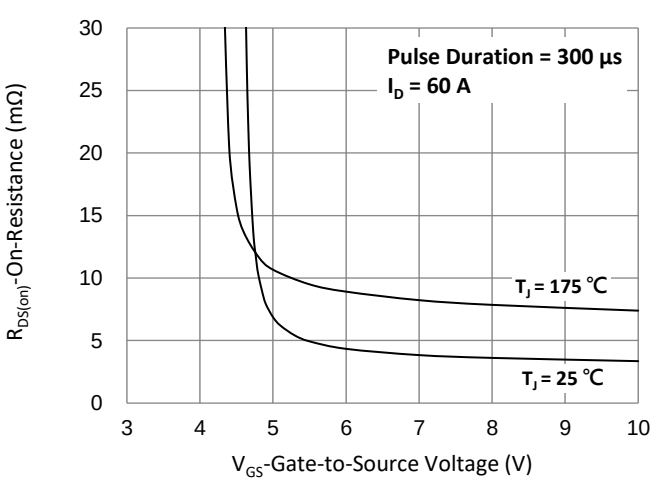


Fig.6 On-Resistance vs. Gate-Source Voltage

TYPICAL CHARACTERISTIC CURVES

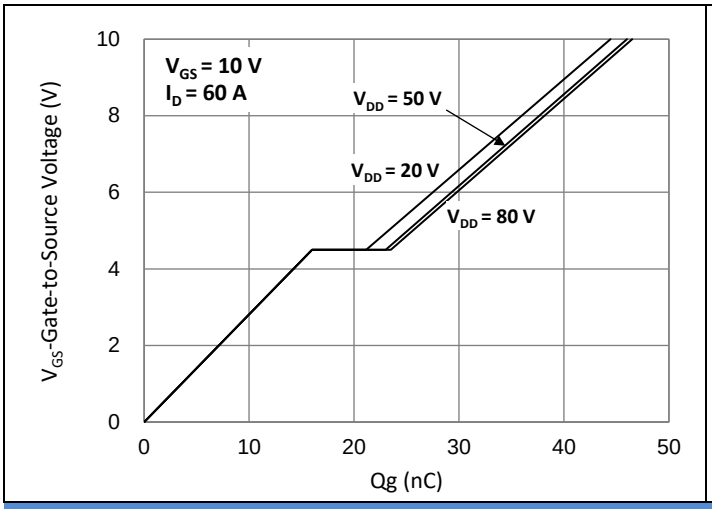


Fig.7 Gate-Charge Characteristics

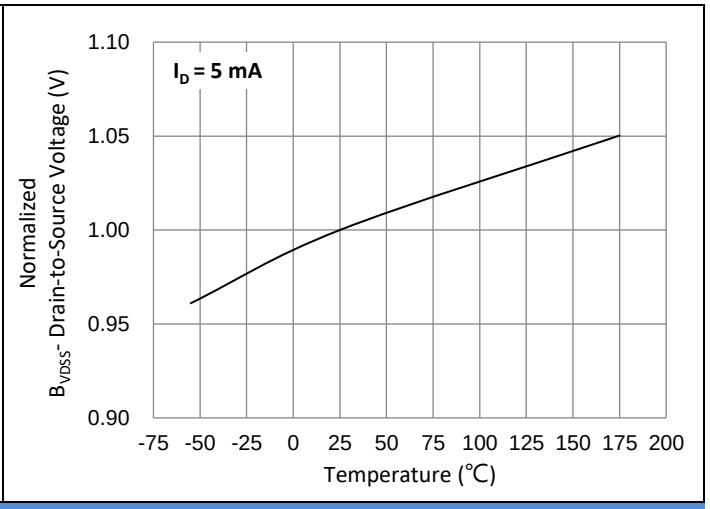


Fig.8 Breakdown Voltage Variation vs. Temperature

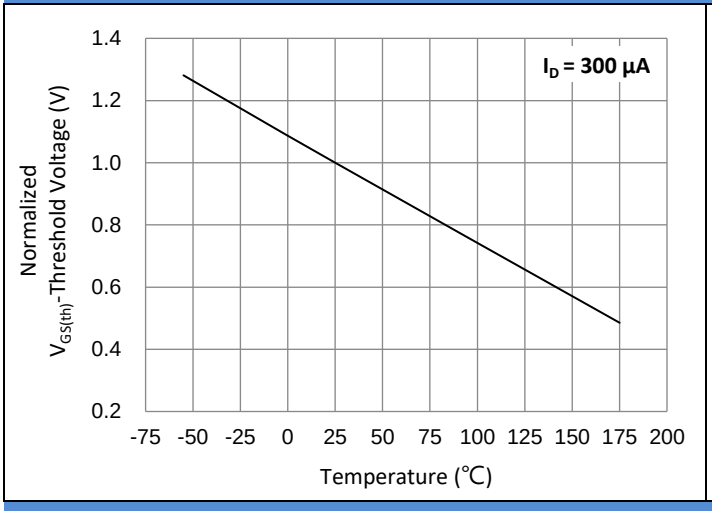


Fig.9 Threshold Voltage Variation with Temperature

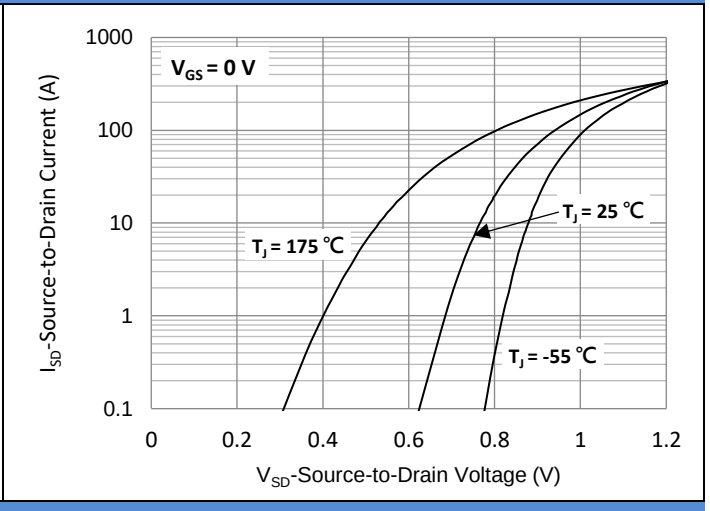


Fig.10 Source-Drain Diode Forward Voltage

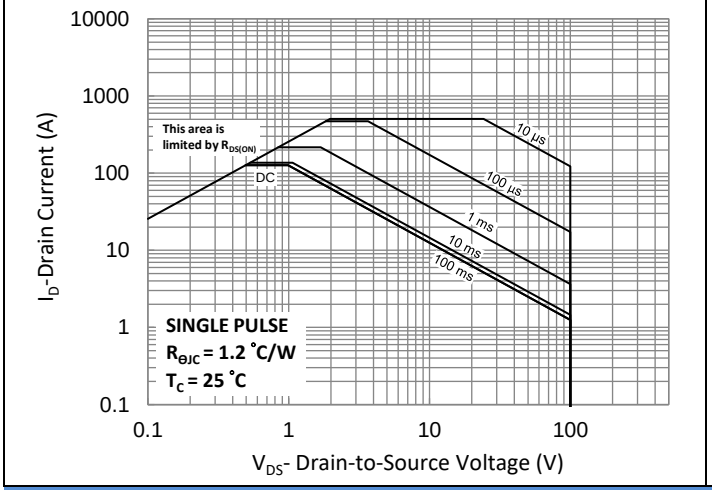


Fig.11 Maximum Safe Operating Area

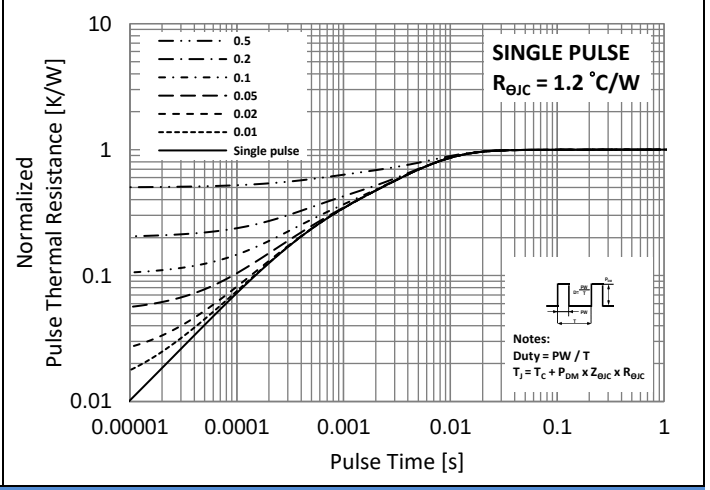


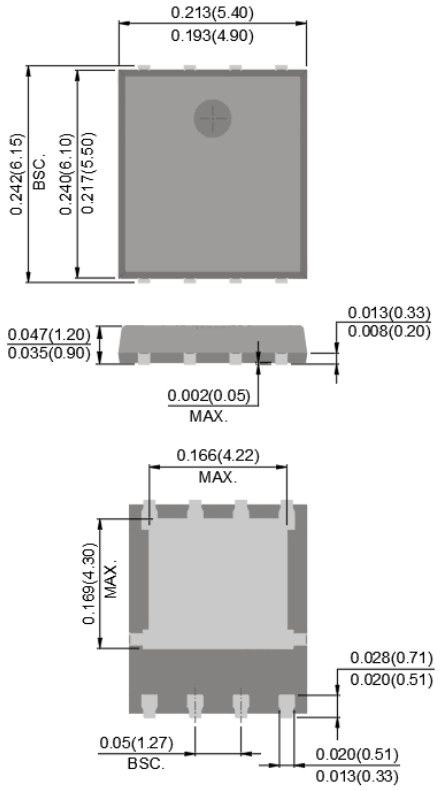
Fig.12 Normalized Transient Thermal Impedance

Product and Packing Information

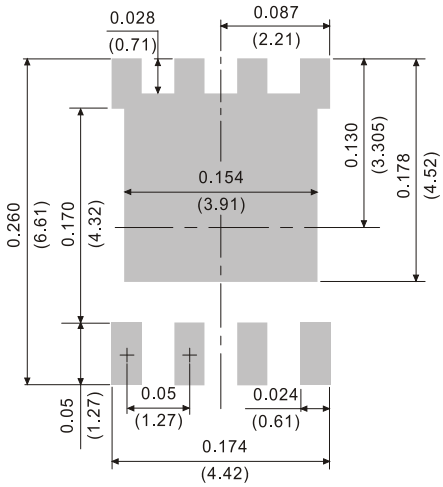
Part No.	Package Type	Packing Type	Marking
PSMQC039N10NS2	DFN5060X-8L	3000pcs / 13” reel	039N10NS

Packaging Information & Mounting Pad Layout

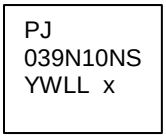
DFN5060X-8L Dimension — Unit: inch(mm)



DFN5060X-8L Pad Layout — Unit: inch(mm)



Marking Diagram



Y = Year Code
W = Week Code (A~Z)
LL = Lot Code (00~99)
x = Production Line Code

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