



PJC7404

20V N-Channel Enhancement Mode MOSFET – ESD Protected

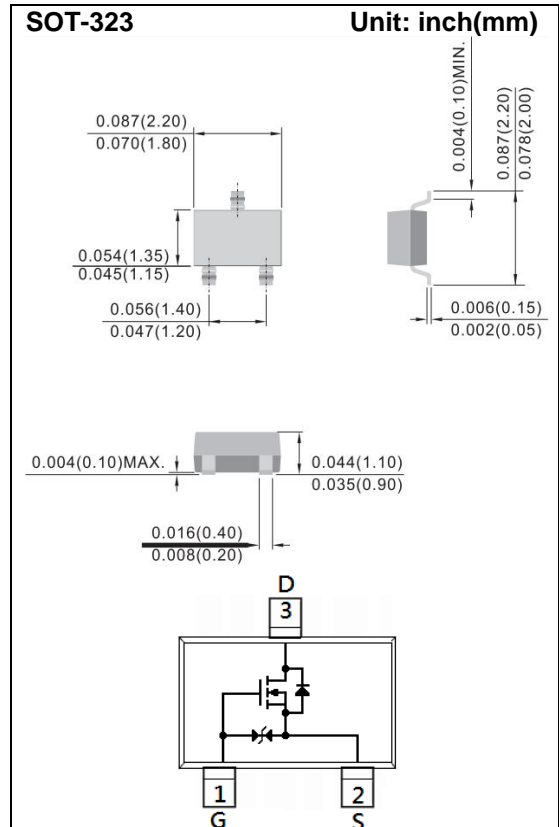
Voltage	20 V	Current	1A
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Features

- RDS(ON) , VGS@4.5V, ID@1.0A<150mΩ
- RDS(ON) , VGS@2.5V, ID@0.7A<215mΩ
- RDS(ON) , VGS@1.8V, ID@0.3A<400mΩ
- Advanced Trench Process Technology
- Specially Designed for Switch Load, PWM Application, etc.
- ESD Protected 2KV HBM
- Lead free in compliance with EU RoHS 2011/65/EU directive
- Green molding compound as per IEC61249 Std.
(Halogen Free)

Mechanical Data

- Case: SOT-323 Package
- Terminals: Solderable per MIL-STD-750, Method 2026
- Approx. Weight: 0.0002 ounces, 0.005 grams
- Marking: C04



Maximum Ratings and Thermal Characteristics (T_A=25 °C unless otherwise noted)

PARAMETER	SYMBOL	LIMIT	UNITS
Drain-Source Voltage	V _{DS}	20	V
Gate-Source Voltage	V _{GS}	±8	V
Continuous Drain Current	I _D	1	A
Pulsed Drain Current (Note 4)	I _{DM}	4	A
Power Dissipation	P _D	T _a =25°C	350 mW
		Derate above 25°C	2.8 mW/°C
Operating Junction and Storage Temperature Range	T _J , T _{STG}	-55~150	°C
Typical Thermal resistance	R _{θJA}	357	°C/W
- Junction to Ambient (Note 3)			



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Electrical Characteristics ($T_A=25^\circ\text{C}$ unless otherwise noted)

PARAMETER	SYMBOL	TEST CONDITION	MIN.	TYP.	MAX.	UNITS
Static						
Drain-Source Breakdown Voltage	BV_{DSS}	$V_{GS}=0V, I_D=250\mu A$	20	-	-	V
Gate Threshold Voltage	$V_{GS(th)}$	$V_{DS}=V_{GS}, I_D=250\mu A$	0.5	0.8	1.0	V
Drain-Source On-State Resistance	$R_{DS(on)}$	$V_{GS}=4.5V, I_D=1A$	-	114	150	m Ω
		$V_{GS}=2.5V, I_D=0.7A$	-	160	215	
		$V_{GS}=1.8V, I_D=0.3A$	-	280	400	
Zero Gate Voltage Drain Current	I_{DSS}	$V_{DS}=20V, V_{GS}=0V$	-	0.01	1	μA
Gate-Source Leakage Current	I_{GSS}	$V_{GS}=\pm 8V, V_{DS}=0V$	-	± 2	± 10	μA
Dynamic						
Total Gate Charge	Q_g	$V_{DS}=10V, I_D=1A,$ $V_{GS}=4.5V$ (Note 1,2)	-	1.6	-	nC
Gate-Source Charge	Q_{gs}		-	0.3	-	
Gate-Drain Charge	Q_{gd}		-	0.41	-	
Input Capacitance	C_{iss}	$V_{DS}=10V, V_{GS}=0V,$ $f=1.0\text{MHZ}$	-	92	-	pF
Output Capacitance	C_{oss}		-	25	-	
Reverse Transfer Capacitance	C_{rss}		-	9.1	-	
Switching						
Turn-On Delay Time	$t_{d(on)}$	$V_{DD}=10V, I_D=1A,$ $V_{GS}=4.5V,$ $R_G=6\Omega$ (Note 1,2)	-	5.8	-	ns
Turn-On Rise Time	t_r		-	25.7	-	
Turn-Off Delay Time	$t_{d(off)}$		-	41	-	
Turn-Off Fall Time	t_f		-	31	-	
Drain-Source Diode						
Maximum Continuous Drain-Source Diode Forward Current	I_S	---	-	-	1	A
Diode Forward Voltage	V_{SD}	$I_S=1A, V_{GS}=0V$	-	0.85	1.2	V

NOTES :

1. Pulse width $\leq 300\mu s$, Duty cycle $\leq 2\%$.
2. Essentially independent of operating temperature typical characteristics.
3. $R_{\theta JA}$ is the sum of the junction-to-case and case-to-ambient thermal resistance where the case thermal reference is defined as the solder mounting surface of the drain pins mounted on a 1 inch FR-4 with 2oz. square pad of copper.
4. The maximum current rating is package limited.



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TYPICAL CHARACTERISTIC CURVES

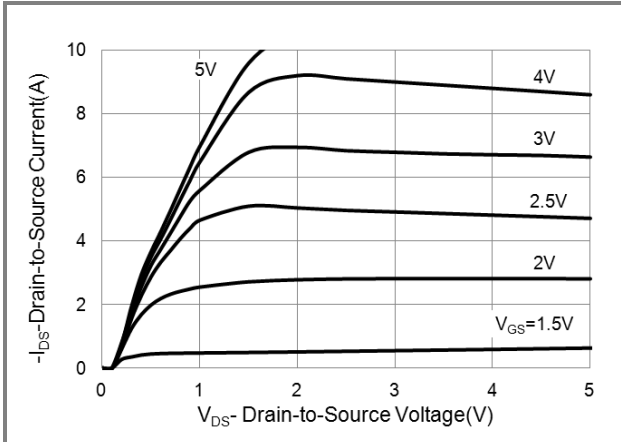


Fig.1 On-Region Characteristics

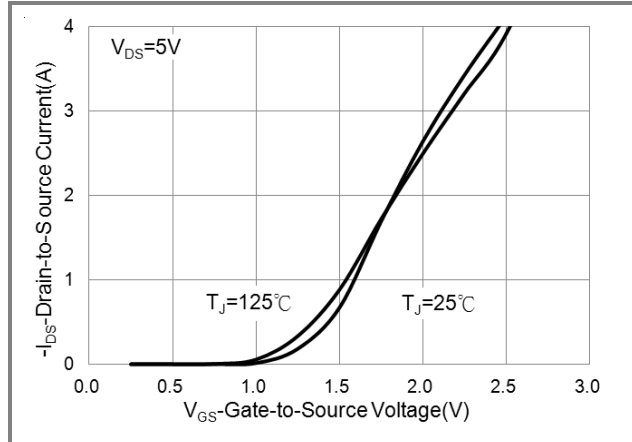


Fig.2 Transfer Characteristics

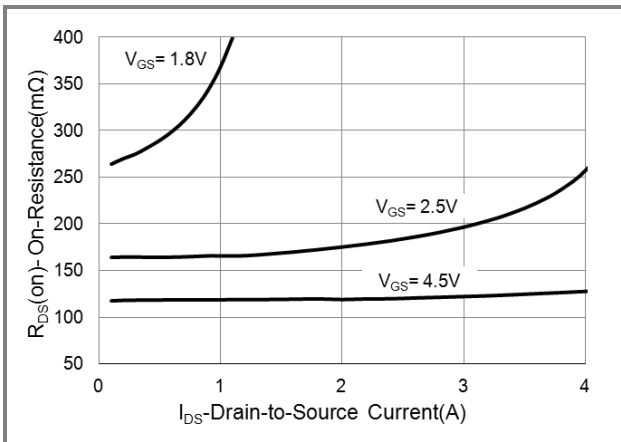


Fig.3 On-Resistance vs. Drain Current

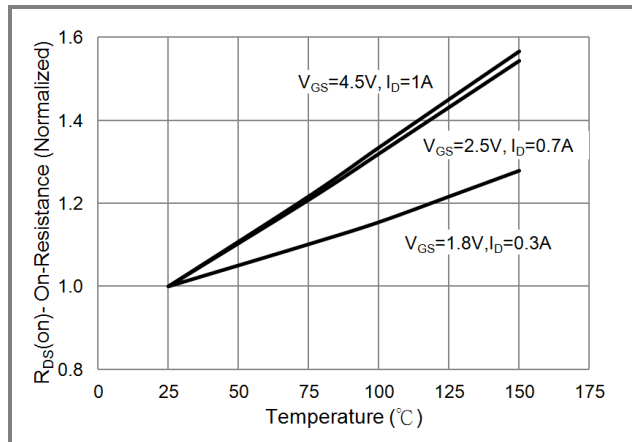


Fig.4 On-Resistance vs. Junction temperature

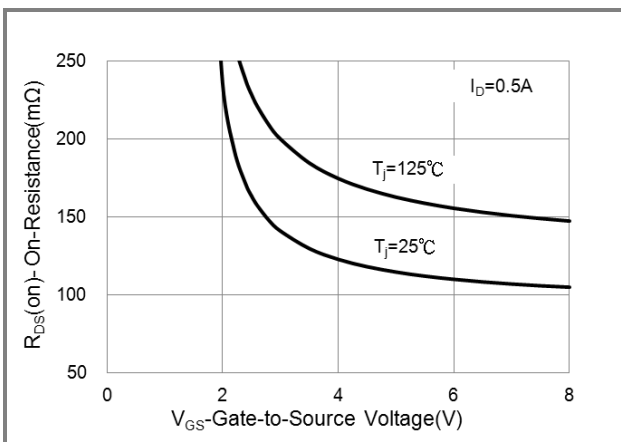


Fig.5 On-Resistance Variation with VGS.

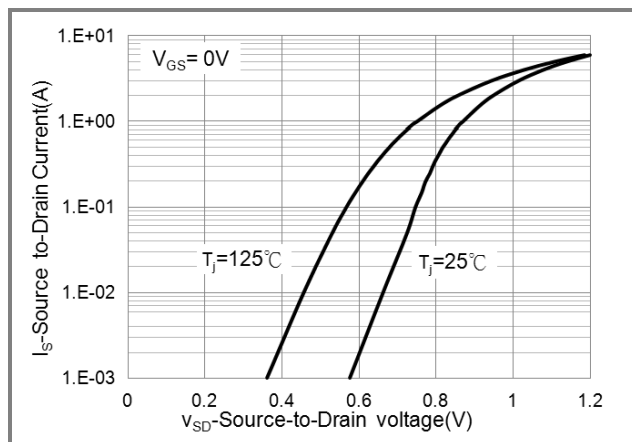


Fig.6 Body Diode Characteristics



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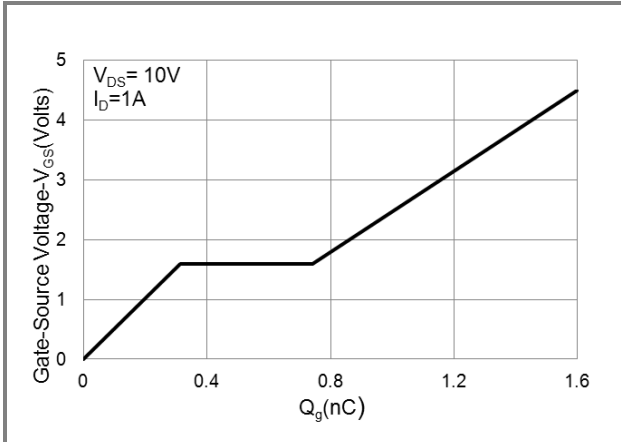


Fig.7 Gate-Charge Characteristics

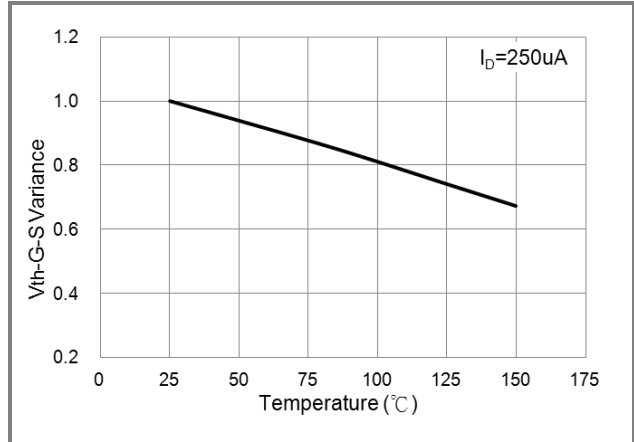


Fig.8 Threshold Voltage Variation with Temperature.

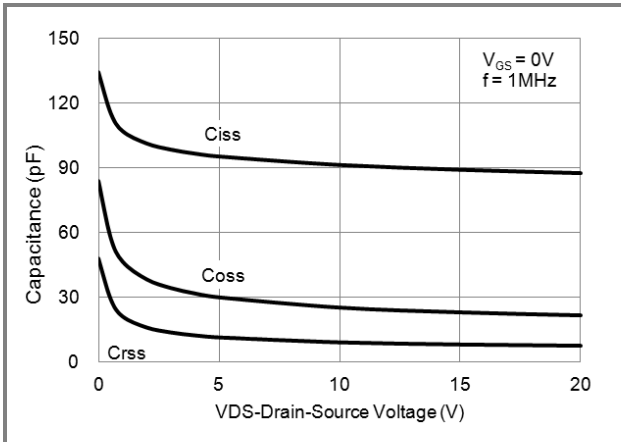


Fig.9 Capacitance vs. Drain-Source Voltage.

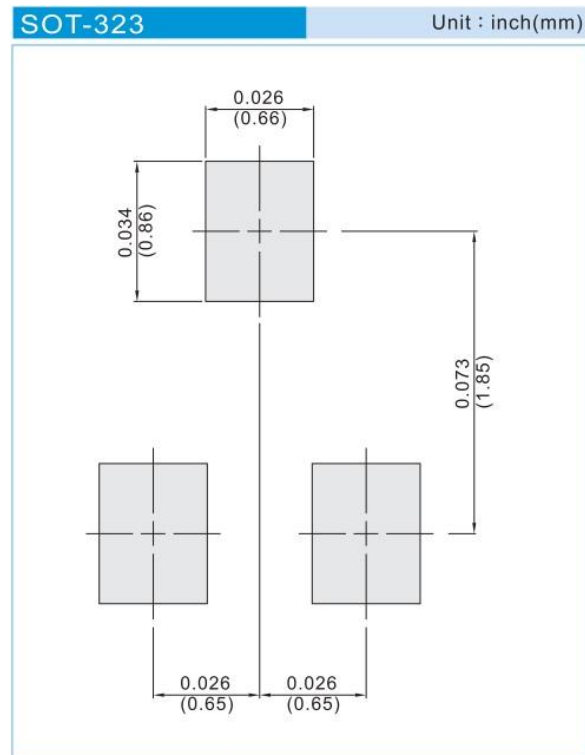


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PART NO PACKING CODE VERSION

Part No Packing Code	Package Type	Packing type	Marking	Version
PJC7404_R1_00001	SOT-323	3K pcs / 7" reel	C04	Halogen free
PJC7404_R2_00001	SOT-323	12K pcs / 13" reel	C04	Halogen free

MOUNTING PAD LAYOUT





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