

# PS2405-D63

## Low Capacitance ESD Protection

**Voltage**

**5V**

### Features

- IEC61000-4-2(ESD) :  $\pm 24$ kV Air,  $\pm 20$ kV Contact
- IEC61000-4-4(EFT) : 40A(5/50ns)
- IEC61000-4-5(Lightning) : 7A (8/20uS)
- Ultra-Low Capacitance: 0.42pF
- Low leakage current, maximum of 0.5uA at rated voltage
- Low clamping voltage
- Lead free in compliance with EU RoHS 2.0
- Green molding compound as per IEC 61249 standard

### Mechanical Data

- Case : DFN1006-3L Package
- Terminals : Solderable per MIL-STD-750, Method 2026
- Approx. Weight : 0.0007 grams

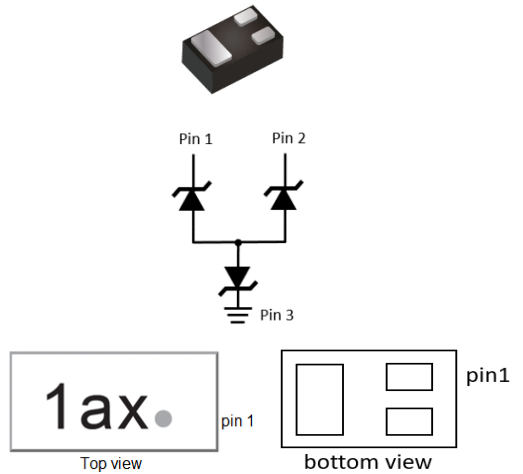
### Applications

- USB 2.0 and 3.0/3.1/3.2
- Notebooks
- SATA ports

### Maximum Ratings and Thermal Characteristics (T<sub>A</sub> = 25°C unless otherwise noted)

PARAMETER	SYMBOL	LIMIT	UNITS
ESD IEC61000-4-2(Air)	V <sub>ESD</sub>	$\pm 24$	kV
ESD IEC61000-4-2(Contact)		$\pm 20$	
Operating Junction Temperature Range	T <sub>J</sub>	-55~125	°C
Storage Temperature Range	T <sub>STG</sub>	-55~150	°C

### DFN1006-3L



Part Marking	Parameter
1ax	1a = Marking Code
	x = Tracking Code

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## Electrical Characteristics (T<sub>A</sub> = 25°C unless otherwise noted)

PARAMETER	SYMBOL	TEST CONDITION	MIN	TYP	MAX	UNITS
Reverse Stand-Off Voltage (Note 1)	V <sub>RWM</sub>	any I/O Pin to GND	-	-	5	V
Reverse Breakdown Voltage	V <sub>BR</sub>	I <sub>BR</sub> = 1mA, any I/O Pin to GND	6	-	12	V
Reverse Leakage Current	I <sub>R</sub>	V <sub>RWM</sub> = 5V, any I/O Pin to GND	-	0.4	0.5	uA
Surge Clamping Voltage (8/20 us)	V <sub>CL</sub>	I <sub>PP</sub> = 5A, any I/O Pin to GND	-	3	4	V
Clamping Voltage TLP (t <sub>period</sub> =100ns,t <sub>r</sub> =1ns) <sup>(Note 2)</sup>	V <sub>CL</sub>	I <sub>TLP</sub> = 16A, any I/O Pin to GND	-	4.5	-	V
Off State Junction Capacitance (Note 3)	C <sub>J</sub>	V <sub>R</sub> = 2.5V, f = 1MHz, any I/O Pin to GND	-	0.39	0.44	pF

**NOTES :**

1. A transient suppressor is selected according to the working peak reverse voltage(V<sub>RWM</sub>), which should be equal to or greater than the DC or continuous peak operation voltage level.
2. Testing using Transmission Line Pulse (TLP) conditions: Z<sub>0</sub> = 50 Ω, t<sub>p</sub> = 100 ns.
3. This parameter is guaranteed by design.
4. This snap-back behavior strongly reduces the clamping voltage to the system behind the ESD protection during an ESD event. Do not connect unlimited DC current sources to the data lines to avoid the ESD protection device maintain in snap-back state after exceeding breakdown voltage.

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## TYPICAL CHARACTERISTIC CURVES

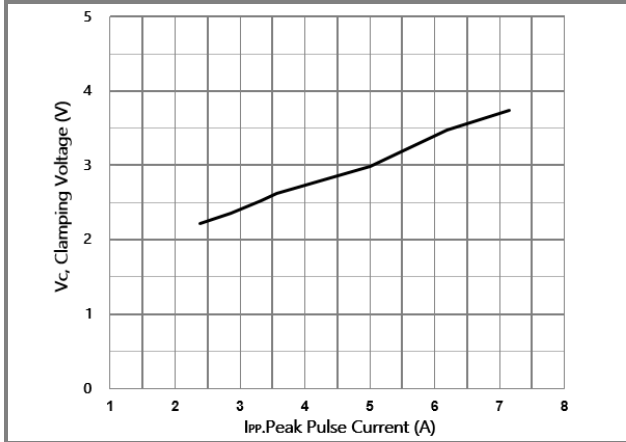


Fig.1 Typical Peak Clamping Voltage

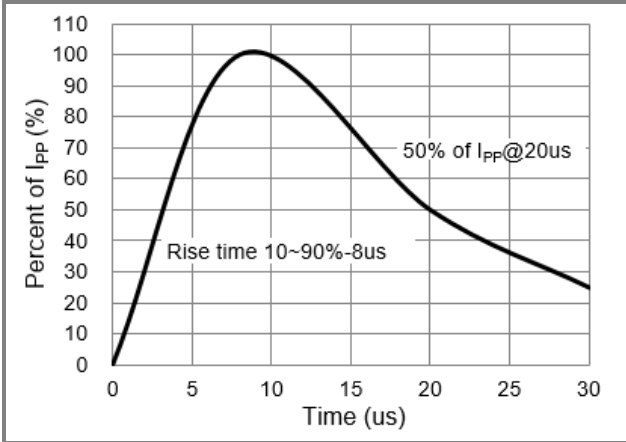


Fig.2 Pulse Waveform

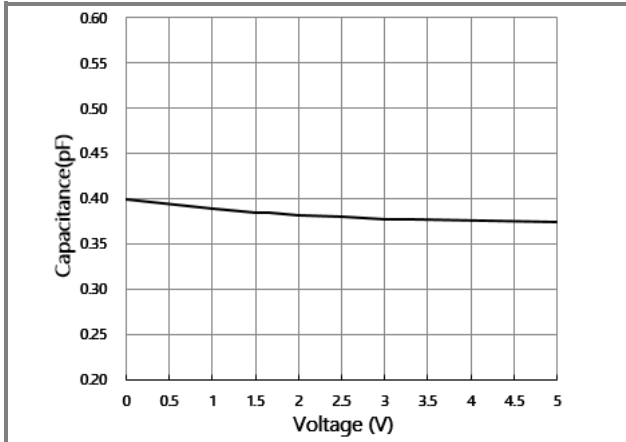


Fig.3 Typical Junction Capacitance

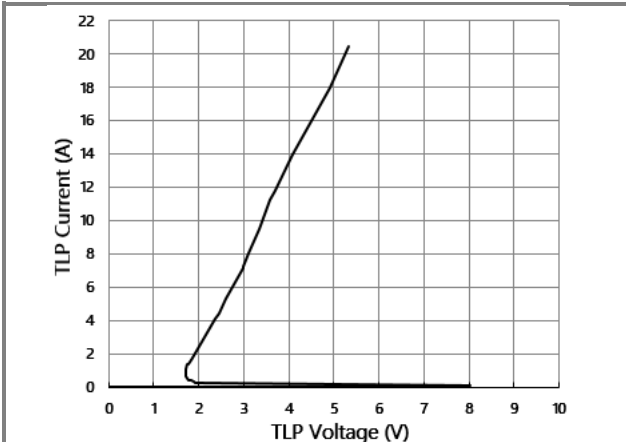


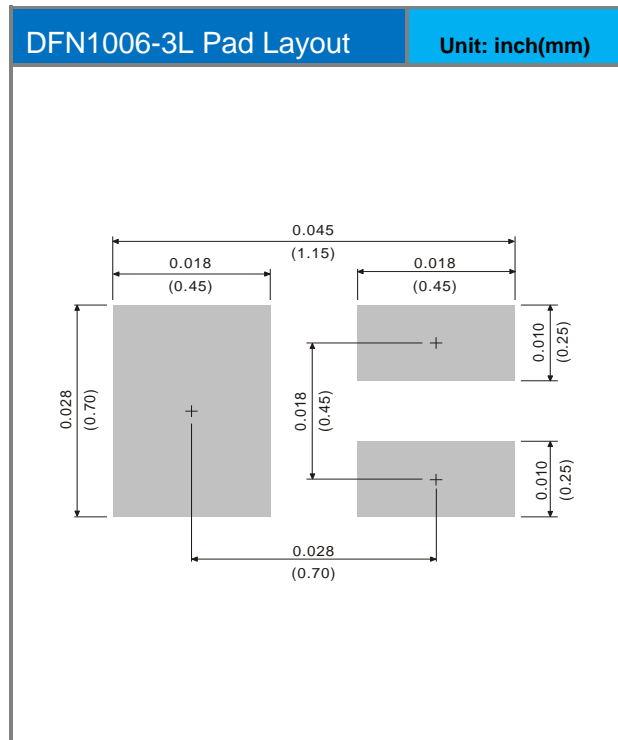
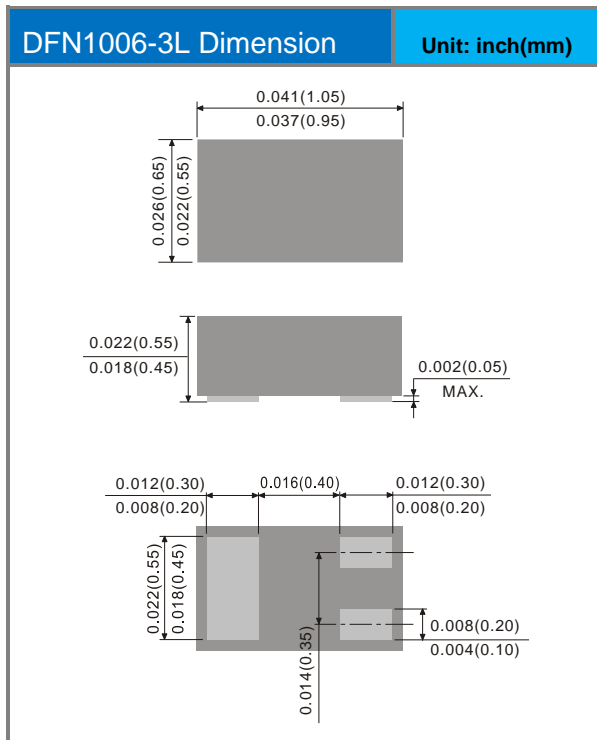
Fig.4 TLP Measurement

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## Product and Packing Information

Part No.	Package Type	Packing Type	Marking
PS2405-D63	DFN1006-3L	10K pcs / 7" reel	1a

## Packaging Information & Mounting Pad Layout



## PS2405-D63

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