

# PS4315-DFA

## Low Capacitance ESD Protection

**Voltage**

**5V**

### Features

- IEC61000-4-2(ESD) : ±15kV Air, ±15kV Contact
- IEC61000-4-4(EFT) : 40A (5/50ns)
- IEC61000-4-5(Lightning) : 6A (8/20uS)
- Low leakage current, maximum of 1uA at rated voltage
- Ultra low clamping voltage
- Lead free in compliance with EU RoHS 2.0
- Green molding compound as per IEC 61249 standard

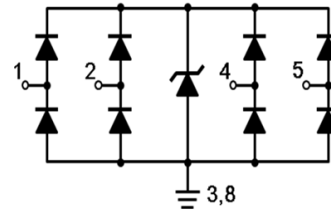
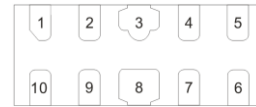
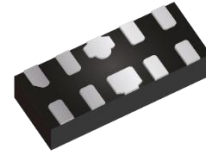
### Mechanical Data

- Case : DFN2510A-10L Package
- Terminals : Solderable per MIL-STD-750, Method 2026
- Approx. Weight : 0.003 grams

### Applications

- USB 3.0, 3.1 and 3.2
- Notebook/Desktop Computers
- SATA/eSATA interface

DFN2510A-10L



**435AYWL**

pin1

Top view

Part Marking	Parameter
435AYWL	435A = Marking Code YWL = Y - Last digit of calendar year W - Weekly L - The latest two digits of wafer lot#

## Maximum Ratings and Thermal Characteristics (T<sub>A</sub> = 25°C unless otherwise noted)

PARAMETER	SYMBOL	VALUE	UNITS
ESD IEC61000-4-2(Air)	V <sub>ESD</sub>	±15	kV
ESD IEC61000-4-2(Contact)		±15	
Operating Junction Temperature Range	T <sub>J</sub>	-55 to +125	°C
Storage Temperature Range	T <sub>STG</sub>	-55 to +150	°C

## PS4315-DFA

### Electrical Characteristics (T<sub>A</sub> = 25°C unless otherwise noted)

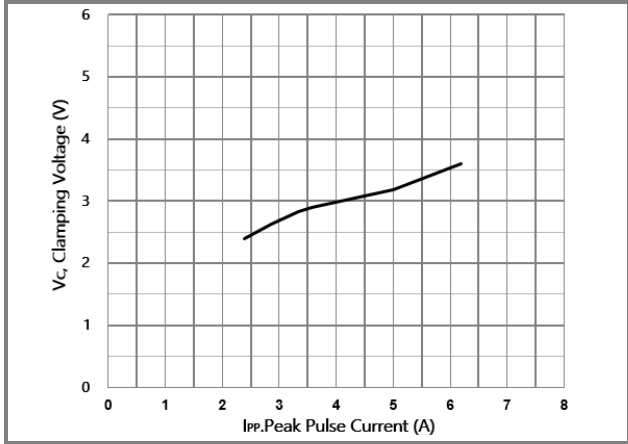
PARAMETER	SYMBOL	TEST CONDITION	MIN.	TYP.	MAX.	UNITS
Reverse Stand-Off Voltage <sup>(Note 1)</sup>	V <sub>RWM</sub>	I/O Pin to GND	-	-	5	V
Reverse Breakdown Voltage	V <sub>BR</sub>	I <sub>BR</sub> = 1mA, I/O Pin to GND	5.5	-	10.5	V
Forward Voltage	V <sub>F</sub>	I <sub>F</sub> = 15mA, I/O Pin to GND	-	1	-	V
Reverse Leakage Current	I <sub>R</sub>	V <sub>R</sub> = 5V, I/O Pin to GND	-	0.5	1	uA
Clamping Voltage	V <sub>CL</sub>	I <sub>PP</sub> = 5A, t <sub>P</sub> = 8/20μs, I/O pins to GND	-	3.2	4.2	V
Clamping Voltage TLP <sup>(Note 2)</sup>	V <sub>CL</sub>	I <sub>PP</sub> = 16A, t <sub>P</sub> = 100ns, I/O Pin to GND	-	4.3	-	V
Off State Junction Capacitance <sup>(Note 3)</sup>	C <sub>J</sub>	2.5Vdc Bias, f = 1MHz, I/O Pins to GND	-	0.29	0.34	pF

NOTES :

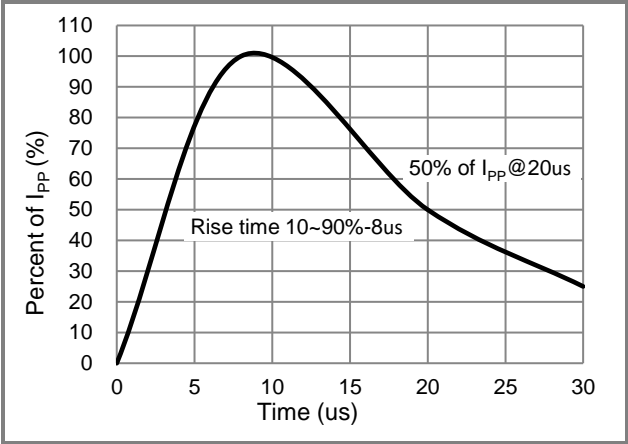
1. A transient suppressor is selected according to the working peak reverse voltage(V<sub>RWM</sub>), which should be equal to or greater than the DC or continuous peak operation voltage level.
2. Testing using Transmission Line Pulse (TLP) conditions: Z<sub>0</sub> = 50Ω, t<sub>P</sub> = 100 ns.
3. This parameter is guaranteed by design.

# PS4315-DFA

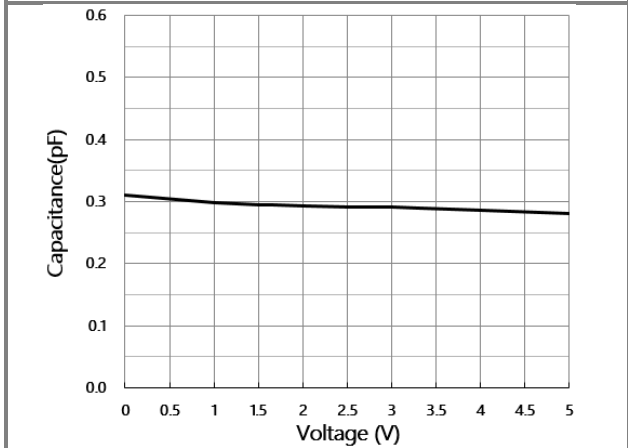
## TYPICAL CHARACTERISTIC CURVES



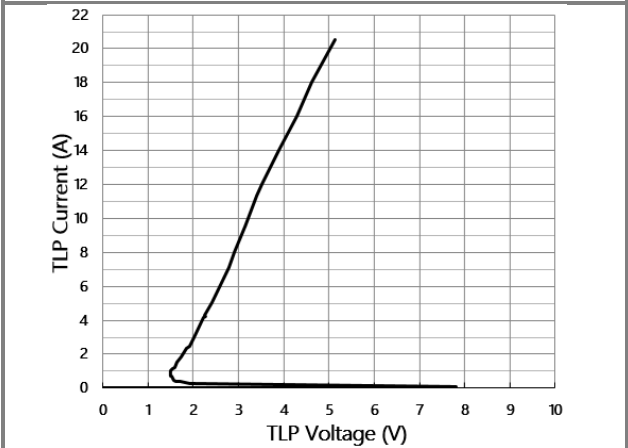
**Fig.1 Typical Peak Clamping Voltage**



**Fig.2 Pulse Waveform**



**Fig.3 Typical Junction Capacitance**



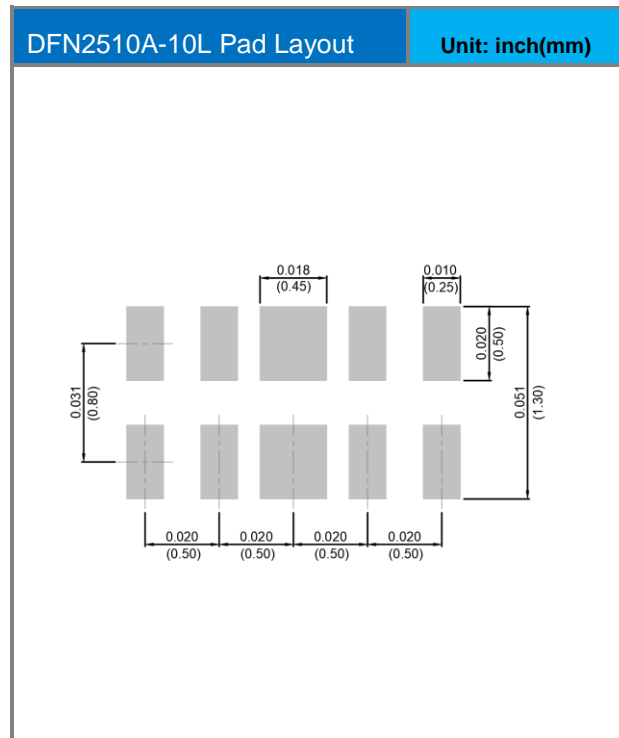
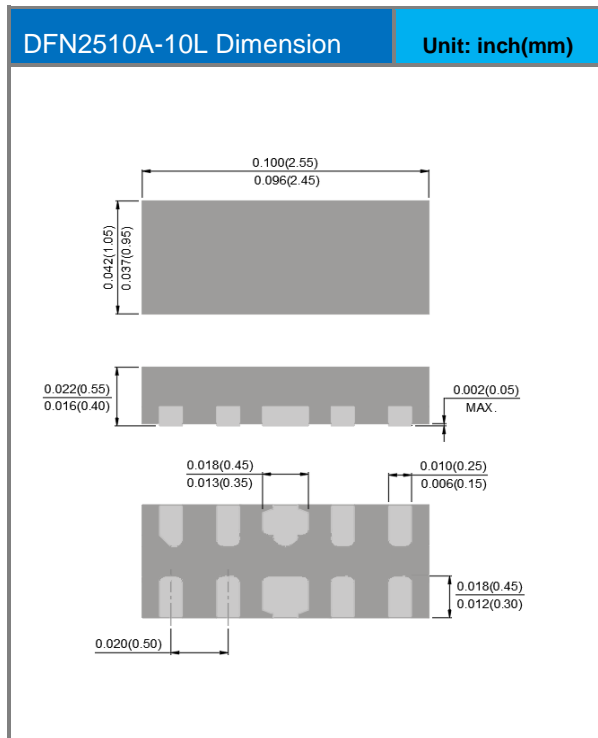
**Fig.4 TLP Measurement**

# PS4315-DFA

## Product and Packing Information

Part No.	Package Type	Packing Type	Marking
PS4315-DFA	DFN2510A-10L	3K pcs / 7" reel	435A

## Packaging Information & Mounting Pad Layout



## PS4315-DFA

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