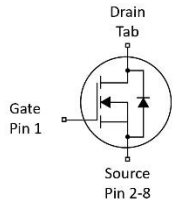
100V N-Channel Enhancement Mode MOSFET

Voltage	**100 V**	**R_{DSON}**	**1.5 mΩ**
Current	**398 A**	**$Q_{G\ (TYP)}$**	**128 nC**

TOLL



Top side view

Feature

- $R_{DS(ON)}$ < 1.5 mΩ at V_{GS} = 10 V, I_D = 100 A
- $R_{DS(ON)}$ < 2.4 mΩ at V_{GS} = 6 V, I_D = 50 A
- High switching speed
- Low reverse transfer capacitance
- Lead free in compliance with EU RoHS 2.0
- Green molding compound as per IEC 61249 standard
- 100% UIS / Rg test in mass production

Mechanical Data

- Case: TOLL Package
- Approx. Weight: 0.775 grams

Application

- ESS / BBU/ LEV / BSG.

Absolute Maximum Ratings (T_A = 25 °C unless otherwise specified)

PARAMETER		SYMBOL	LIMIT	UNITS
Drain-Source Voltage		V_{DS}	100	V
Gate-Source Voltage		V_{GS}	±20	
Continuous Drain Current by $R_{\theta JC}$ (Note 3)	T_C=25 °C	I_D	398	A
	T_C=100 °C		281	
Continuous Drain Current by $R_{\theta JA}$	T_A=25 °C	I_D	34	A
	T_A=70 °C		28	
Pulsed Drain Current by $R_{\theta JC}$	T_C=25 °C	I_{DM}	1592	A
Single Pulse Avalanche Current (Note 5)		I_{AS}	80	A
Single Pulse Avalanche Energy (Note 5)		E_{AS}	1152	mJ
Power Dissipation by $R_{\theta JC}$	T_C=25 °C	P_D	500	W
	T_C=100 °C		250	
Power Dissipation by $R_{\theta JA}$	T_A=25 °C	P_D	3.8	W
	T_A=70 °C		2.6	
Operating Junction and Storage Temperature Range		T_J,T_{STG}	-55~175	°C

Thermal Characteristics

PARAMETER		SYMBOL	VALUES			UNITS
			MIN.	TYP.	MAX.	
Thermal Resistance	Junction-to-Case (Bottom)	$R_{\theta JC}$	-	0.18	0.3	°C/W
	Junction-to-Ambient (Note 4)	$R_{\theta JA}$	-	-	40	°C/W

Electrical Characteristics (T_A = 25 °C unless otherwise specified)

PARAMETER	SYMBOL	TEST CONDITION	MIN.	TYP.	MAX.	UNITS
Static Characteristics						
Drain-Source Breakdown Voltage	BV_{DSS}	V_{GS}=0 V, I_D=250 μA	100	-	-	V
Gate Threshold Voltage	$V_{GS(th)}$	V_{DS}=V_{GS}, I_D=890 μA	1.8	2.8	3.8	
Drain-Source On-State Resistance (Note 1)	$R_{DS(on)}$	V_{GS}=10 V, I_D=100 A	-	1.2	1.5	mΩ
		V_{GS}=6 V, I_D=50 A	-	1.6	2.4	
Zero Gate Voltage Drain Current	I_{DSS}	V_{DS}=100 V, V_{GS}=0 V	-	-	5	μA
Gate-Source Leakage Current	I_{GSS}	V_{GS}=±20 V, V_{DS}=0 V	-	-	±100	nA
Transfer characteristics (Note 1)	g_{fs}	V_{DS}=10 V, I_D=100 A	-	300	-	S
Dynamic Characteristics (Note 6)						
Total Gate Charge	Q_g	V_{DS}=50 V, I_D=100 A, V_{GS}=10 V	-	128	166	nC
Gate-Source Charge	Q_{gs}		-	42	-	
Gate-Drain Charge	Q_{gd}		-	17	-	
Gate Plateau Voltage	$V_{plateau}$		-	4.5	-	V
Input Capacitance	C_{iss}	V_{DS}=50 V, V_{GS}=0 V, f=250 kHz	-	9640	12500	pF
Output Capacitance	C_{oss}		-	3670	4770	
Reverse Transfer Capacitance	C_{rss}		-	39	-	
Output Charge	Q_{oss}	V_{DS}=50 V, V_{GS}=0 V	-	277	360	nC
Turn-On Delay Time	$t_{d(on)}$	V_{DD}=50 V, I_D=100 A, V_{GS}=10 V, R_G=1.8 Ω (Note 2)	-	24.5	-	ns
Rise Time	t_r		-	8.9	-	
Turn-Off Delay Time	$t_{d(off)}$		-	44.8	-	
Fall Time	t_f		-	10.2	-	
Gate Resistance	R_g	f =1.0 MHz	-	0.5	1.0	Ω
Drain-Source Diode						
Diode Forward Voltage	V_{SD}	I_S=100 A, V_{GS}=0 V	-	0.9	1.2	V
Reverse Recovery Charge	Q_{rr}	I_F=100 A, V_{DD}=50 V, di/dt=100 A/μs	-	88	-	nC
Reverse Recovery Time	T_{rr}		-	260	-	ns

NOTES :

1. Pulse width ≤ 300 μs, Duty cycle ≤ 2 %.
2. Essentially independent of operating temperature typical characteristics.
3. The maximum drain current calculated by maximum junction temperature and thermal impedance. It can be varied by application and environment.
4. $R_{\theta JA}$ is the sum of the junction-to-case and case-to-ambient thermal resistance where the case thermal reference is defined as the solder mounting surface of the drain pins. Mounted on a 1 $inch^2$ with 2oz.square pad of copper.
5. E_{AS} is calculated based on the condition of L = 1.0 mH, I_{AS} = 48 A, V_{DD} = 50 V, V_{GS} = 10 V. 100% test at L = 0.1 mH, I_{AS} = 80 A in production.
6. Guaranteed by design, not subject to production testing.

TYPICAL CHARACTERISTIC CURVES

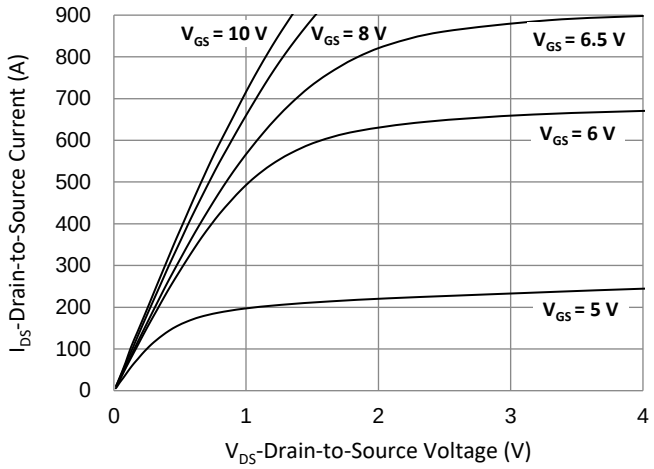


Fig.1 Output Characteristics

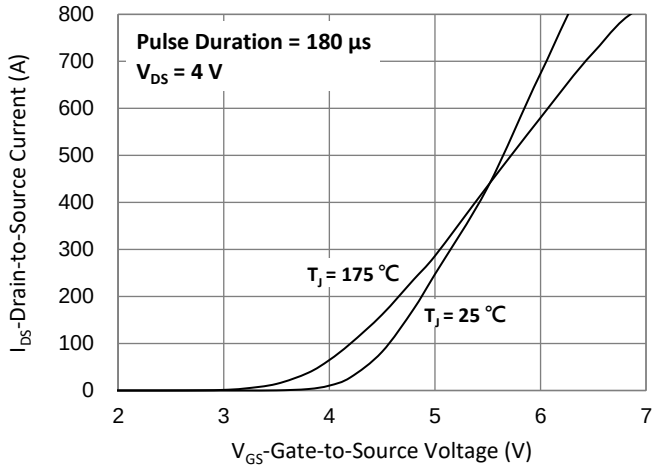


Fig.2 Transfer Characteristics

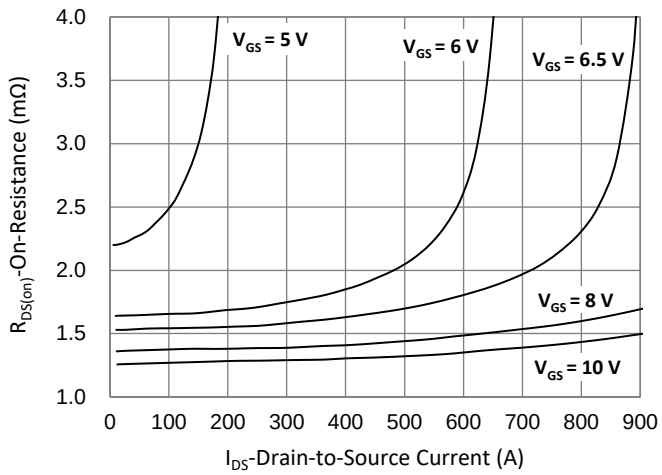


Fig.3 On-Resistance vs. Drain Current

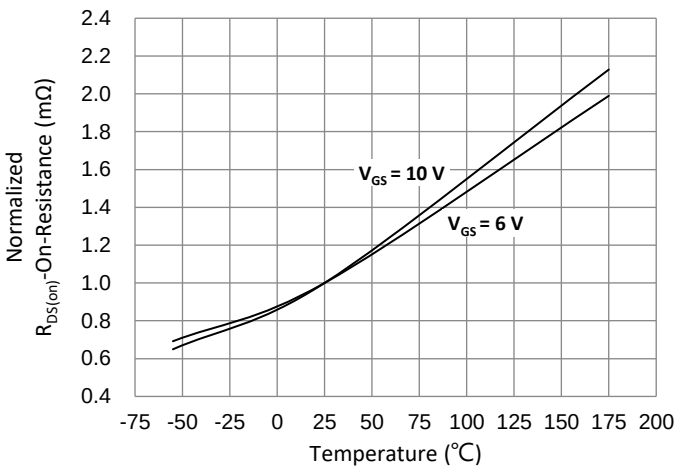


Fig.4 On-Resistance vs. Junction temperature

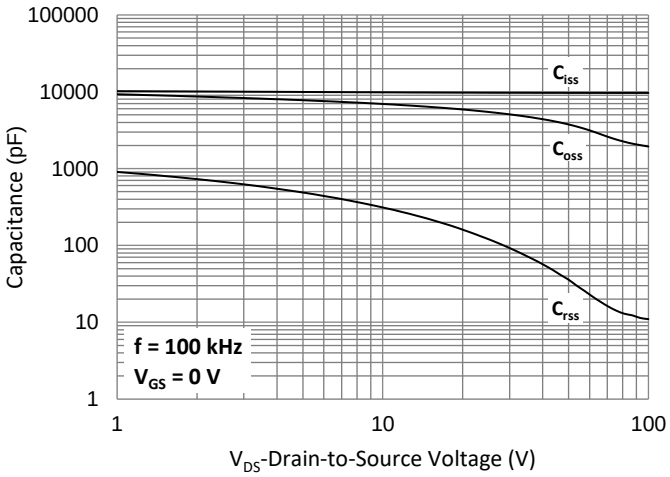


Fig.5 Capacitance vs. Drain-Source Voltage

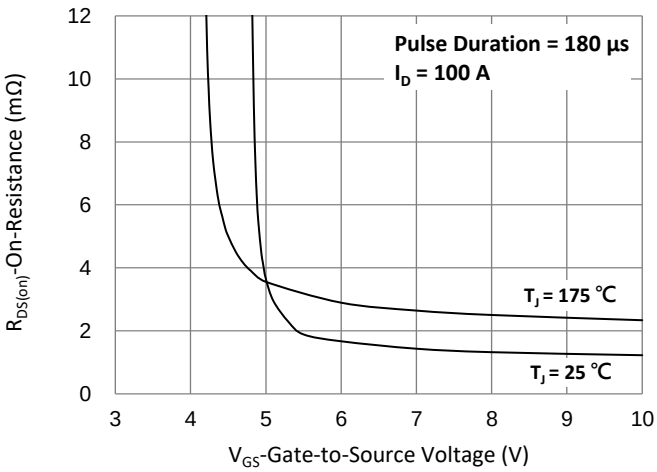


Fig.6 On-Resistance vs. Gate-Source Voltage

TYPICAL CHARACTERISTIC CURVES

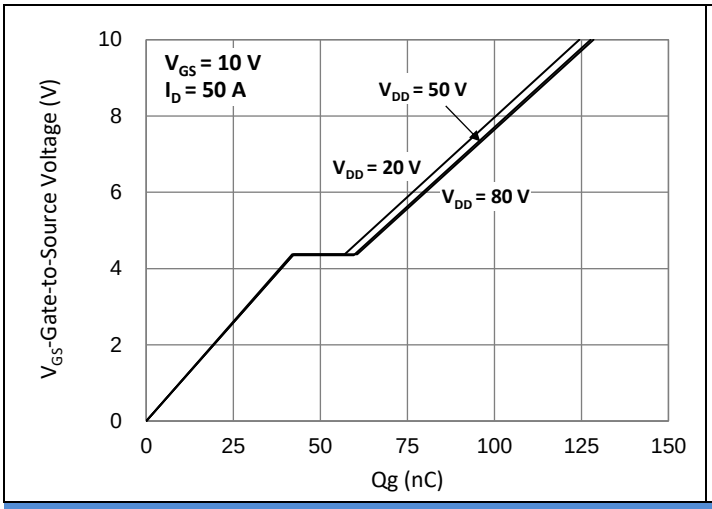


Fig.7 Gate-Charge Characteristics

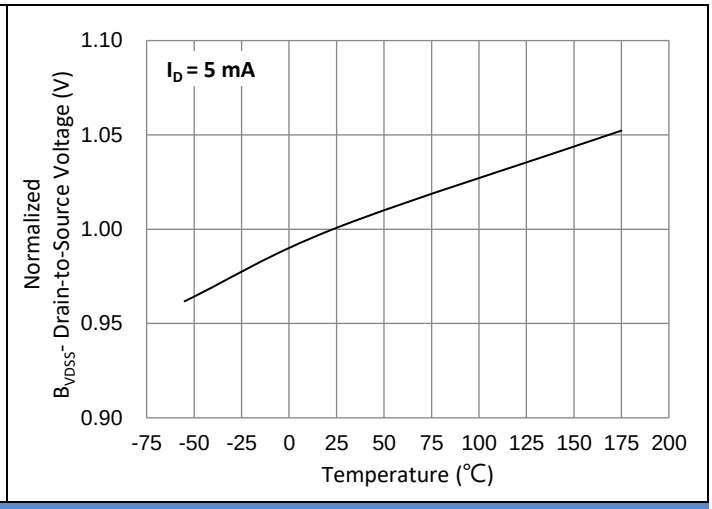


Fig.8 Breakdown Voltage Variation vs. Temperature

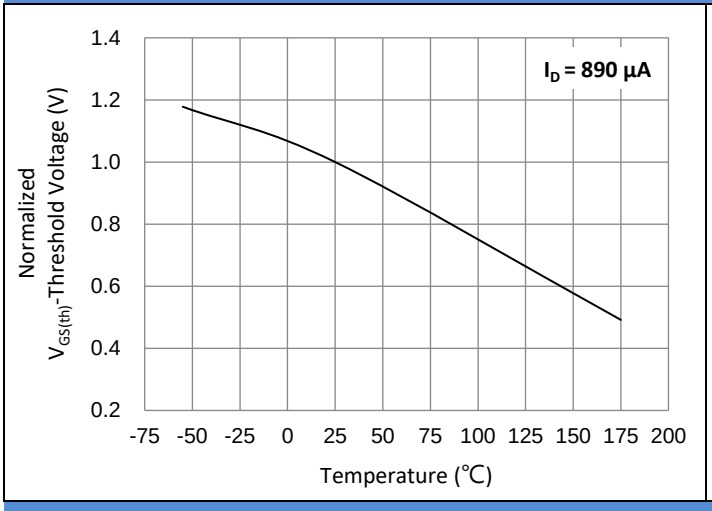


Fig.9 Threshold Voltage Variation with Temperature

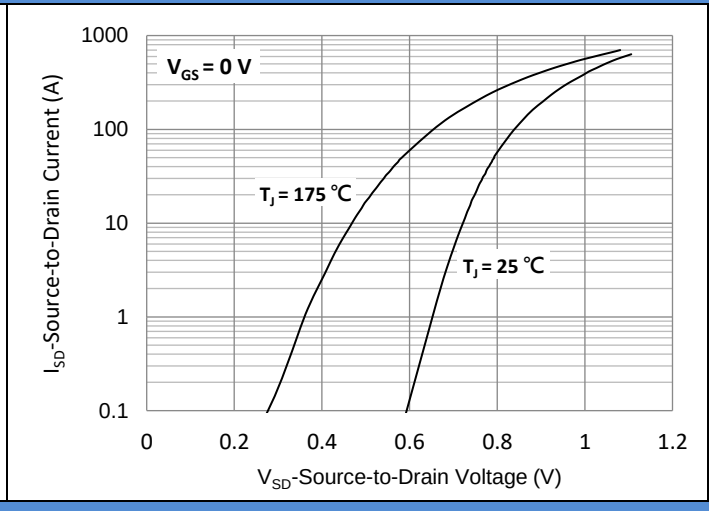


Fig.10 Source-Drain Diode Forward Voltage

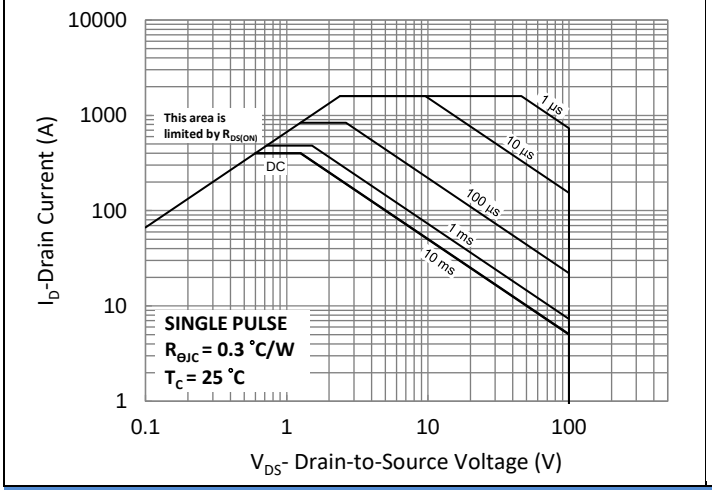


Fig.11 Maximum Safe Operating Area

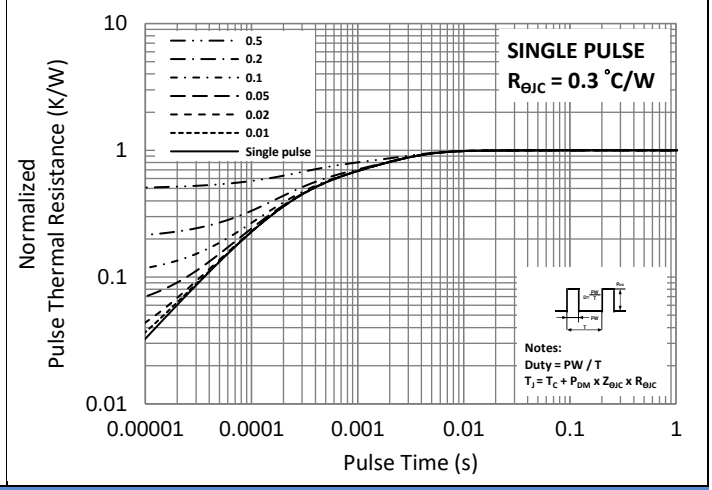


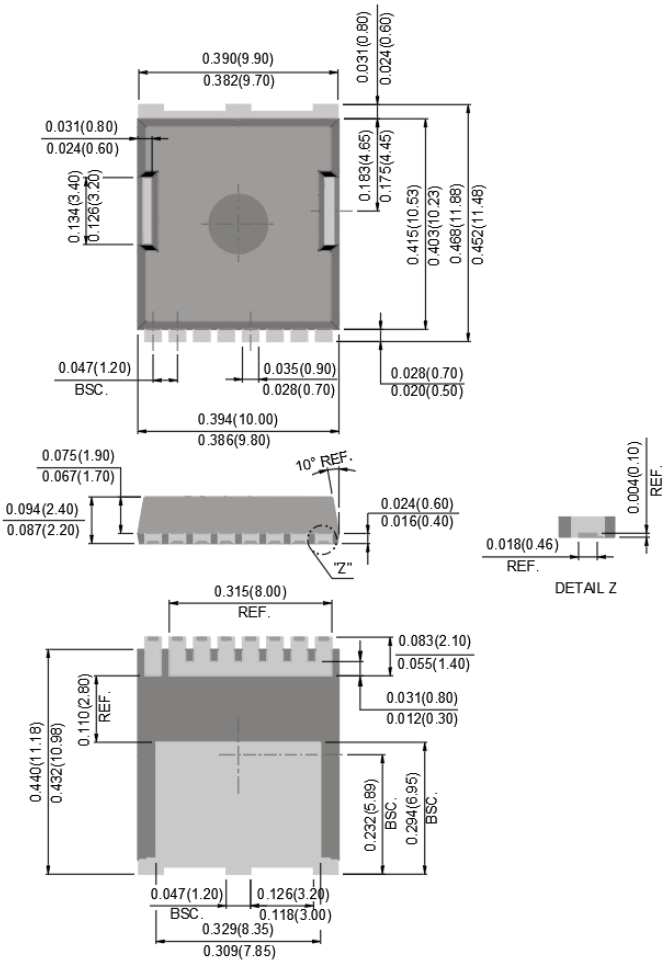
Fig.12 Normalized Transient Thermal Impedance

Product and Packing Information

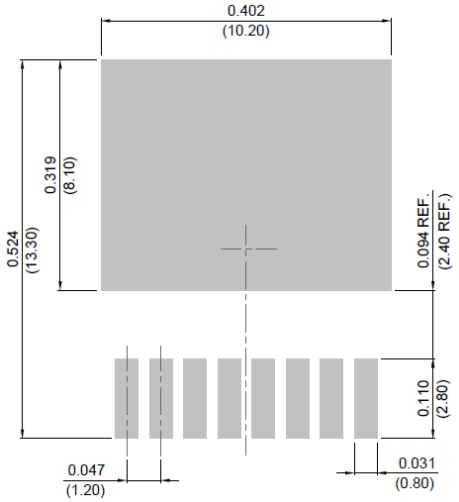
Part No.	Package Type	Packing Type	Marking
PSMN015N10NS2	TOLL	2000pcs / reel	015N10NS

Packaging Information & Mounting Pad Layout

TOLL Dimension — Unit: inch(mm)



TOLL Pad Layout — Unit: inch(mm)



Marking Diagram

PJ
015N10NS
YWLL x

Y = Year Code
W = Week Code (A~Z)
LL = Lot Code (00~99)
x = Production Line Code

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