

80V N-Channel Enhancement Mode MOSFET

Voltage	80 V	R_{DS(ON)}	2.0 mΩ
Current	307 A	Q_G (TYP)	70 nC

Feature

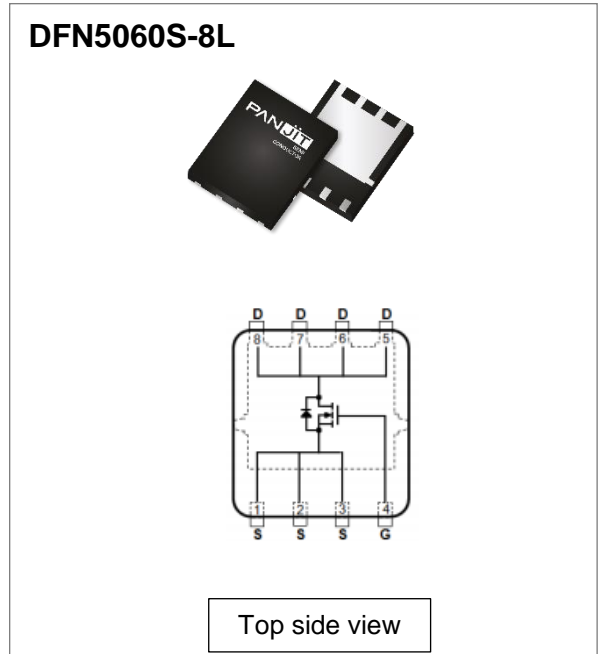
- R_{DS(ON)} < 2.0 mΩ at V_{GS} = 10 V, I_D = 50 A
- R_{DS(ON)} < 3.3 mΩ at V_{GS} = 7 V, I_D = 25 A
- High switching speed
- Low reverse transfer capacitance
- Lead free in compliance with EU RoHS 2.0
- Green molding compound as per IEC 61249 standard
- 100% UIS / Rg test in mass production

Mechanical Data

- Case: DFN5060S-8L Package
- Terminals: Solderable per MIL-STD-750, Method 2026
- Approx. Weight: 0.1168 gram

Application

- Brick Power / Server Power



Absolute Maximum Ratings (T_A = 25 °C unless otherwise specified)

PARAMETER		SYMBOL	LIMIT	UNITS	
Drain-Source Voltage		V _{DS}	80	V	
Gate-Source Voltage		V _{GS}	±20		
Continuous Drain Current (Note 3)	T _C =25 °C	I _D	307	A	
	T _C =100 °C		217		
Pulsed Drain Current		T _C =25 °C	I _{DM}	1226	A
Single Pulse Avalanche Current (Note 5)			I _{AS}	45.5	A
Single Pulse Avalanche Energy (Note 5)			E _{AS}	104	mJ
Power Dissipation	T _C =25 °C	P _D	333	W	
	T _C =100 °C		167		
Operating Junction and Storage Temperature Range		T _J , T _{STG}	-55~175	°C	

Thermal Characteristics

PARAMETER	SYMBOL	VALUES			UNITS	
		MIN.	TYP.	MAX.		
Thermal Resistance	Junction-to-Case (Bottom)	R _{θJC}	-	0.28	0.45	°C/W
	Junction-to-Ambient (Note 4)	R _{θJA}	-	40	-	°C/W

Electrical Characteristics (T_A = 25 °C unless otherwise specified)

PARAMETER	SYMBOL	TEST CONDITION	MIN.	TYP.	MAX.	UNITS
Static Characteristics						
Drain-Source Breakdown Voltage	BV _{DSS}	V _{GS} =0 V, I _D =250 μA	80	-	-	V
Gate Threshold Voltage	V _{GS(th)}	V _{DS} =V _{GS} , I _D =400 μA	1.8	2.8	3.8	
Drain-Source On-State Resistance (Note 1)	R _{DS(on)}	V _{GS} =10 V, I _D =50 A	-	1.6	2.0	mΩ
		V _{GS} = 7 V, I _D =25 A	-	2	3.3	
Zero Gate Voltage Drain Current	I _{DSS}	V _{DS} =80 V, V _{GS} =0 V	-	-	1	μA
Gate-Source Leakage Current	I _{GSS}	V _{GS} =±20 V, V _{DS} =0 V	-	-	±100	nA
Dynamic Characteristics (Note 6)						
Total Gate Charge	Q _g	V _{DS} =40 V, I _D =100 A, V _{GS} =10 V	-	70	91	nC
Gate-Source Charge	Q _{gs}		-	22.2	-	
Gate-Drain Charge	Q _{gd}		-	15.1	-	
Gate Plateau Voltage	V _{plateau}		-	4.6	-	V
Input Capacitance	C _{iss}	V _{DS} =40 V, V _{GS} =0 V, f=250 kHz	-	4577	5950	pF
Output Capacitance	C _{oss}		-	2076	2700	
Reverse Transfer Capacitance	C _{rss}		-	52.3	-	
Output Charge	Q _{oss}	V _{DS} =40 V, V _{GS} =0 V	-	119	154	nC
Turn-On Delay Time	t _{d(on)}	V _{DD} =40 V, I _D =100 A, V _{GS} =10 V, R _G =1.6 Ω (Note 2)	-	19	-	ns
Rise Time	t _r		-	9	-	
Turn-Off Delay Time	t _{d(off)}		-	31.7	-	
Fall Time	t _f		-	12	-	
Gate Resistance	R _g	f =1.0 MHz	-	0.6	1.2	Ω
Drain-Source Diode						
Diode Forward Voltage	V _{SD}	I _S =50 A, V _{GS} =0 V	-	0.9	1.2	V
Reverse Recovery Charge	Q _{rr}	I _F =100 A, V _{DD} =40 V, di/dt=100 A/μs	-	154	-	nC
Reverse Recovery Time	T _{rr}		-	84	-	ns
	T _a		-	45.7	-	ns
	T _b		-	38.1	-	ns

NOTES :

- Pulse width ≤ 560 μs, Duty cycle ≤ 2 %.
- Essentially independent of operating temperature typical characteristics.
- The maximum drain current calculated by maximum junction temperature and thermal impedance. It can be varied by application and environment.
- R_{θJA} is the sum of the junction-to-case and case-to-ambient thermal resistance where the case thermal reference is defined as the solder mounting surface of the drain pins. Mounted on a 1 inch² with 2oz.square pad of copper.
- E_{AS} is calculated based on the condition of L = 0.1 mH, I_{AS} = 55 A, V_{DD} = 40 V, V_{GS} = 10 V. 100% test in production.
- Guaranteed by design, not subject to production testing.

TYPICAL CHARACTERISTIC CURVES

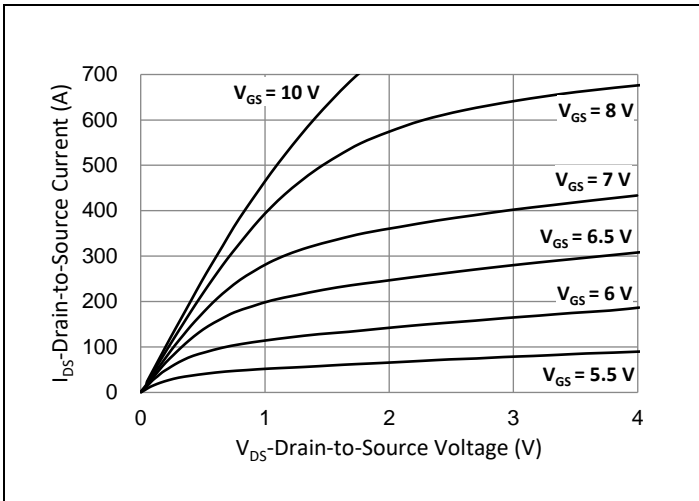


Fig.1 Output Characteristics

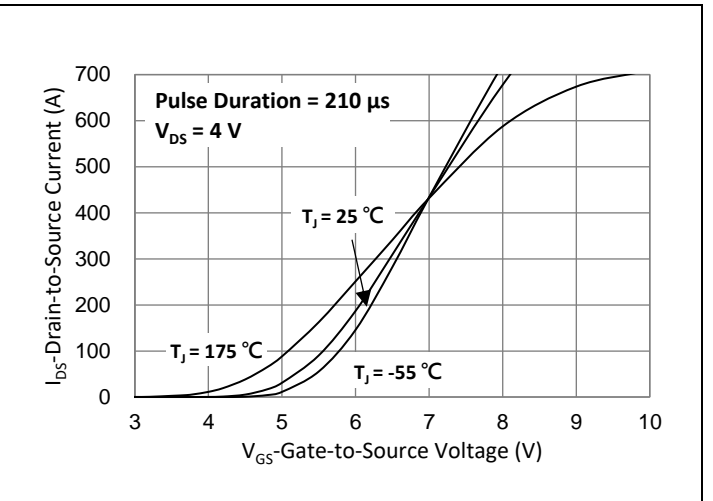


Fig.2 Transfer Characteristics

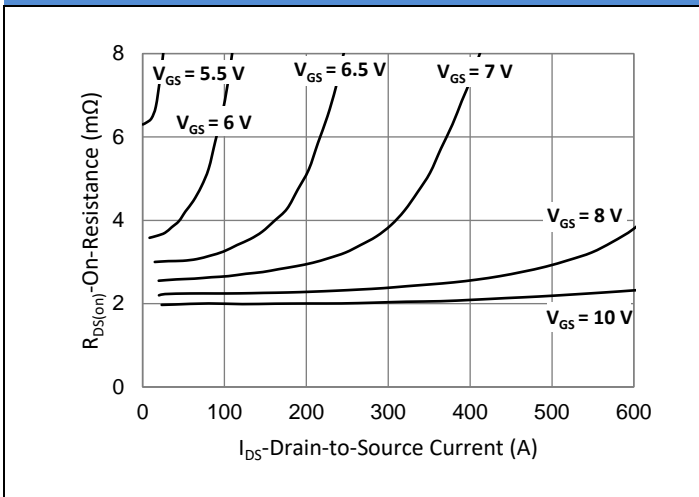


Fig.3 On-Resistance vs. Drain Current

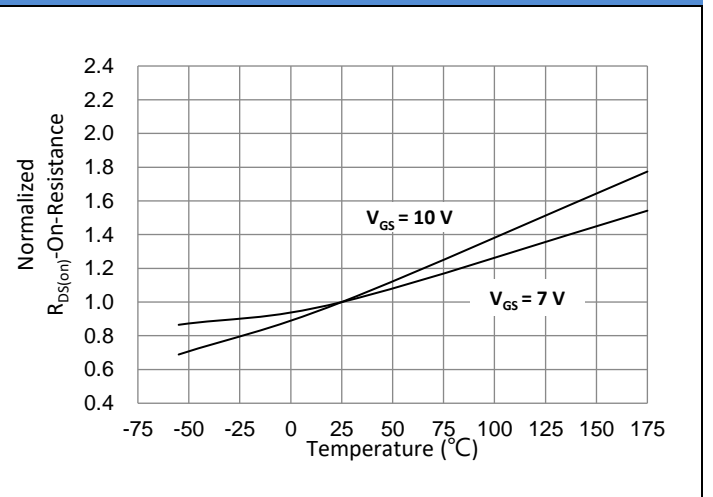


Fig.4 On-Resistance vs. Junction temperature

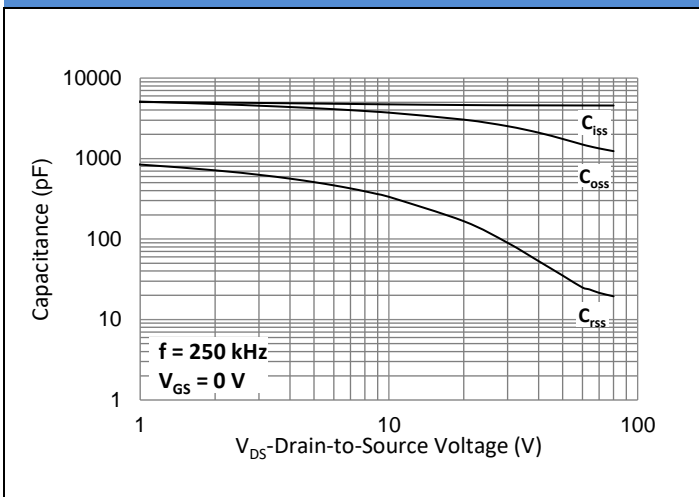


Fig.5 Capacitance vs. Drain-Source Voltage

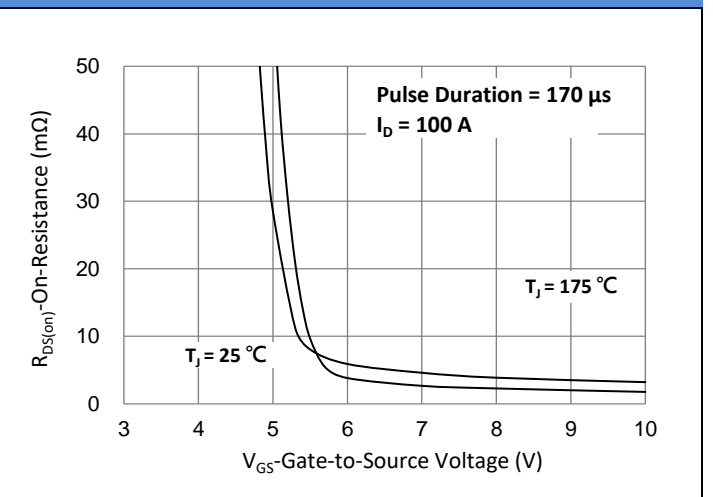


Fig.6 On-Resistance vs. Gate-Source Voltage

TYPICAL CHARACTERISTIC CURVES

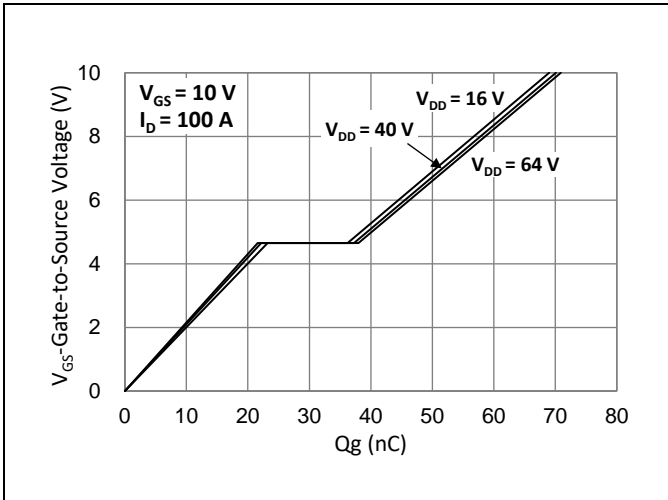


Fig.7 Gate-Charge Characteristics

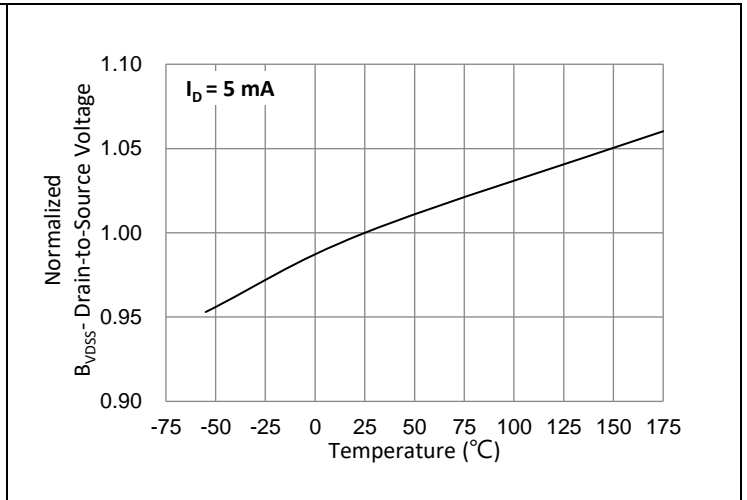


Fig.8 Breakdown Voltage Variation vs. Temperature

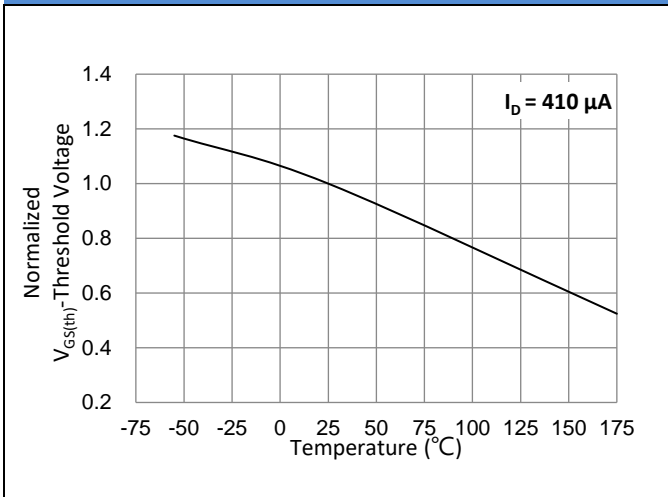


Fig.9 Threshold Voltage Variation with Temperature

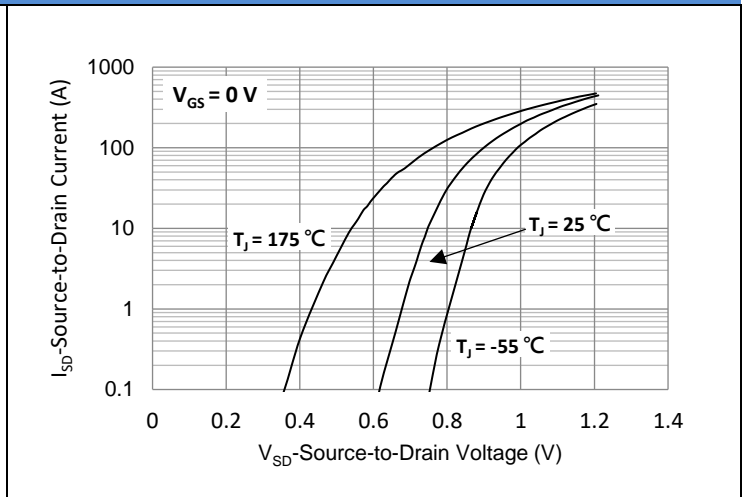


Fig.10 Source-Drain Diode Forward Voltage

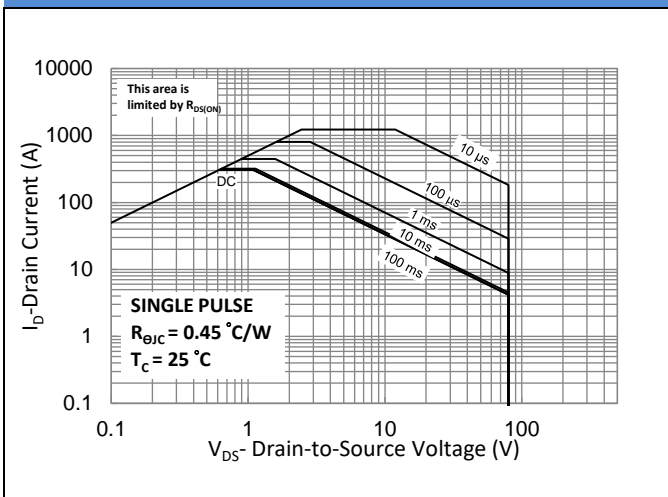


Fig.11 Maximum Safe Operating Area

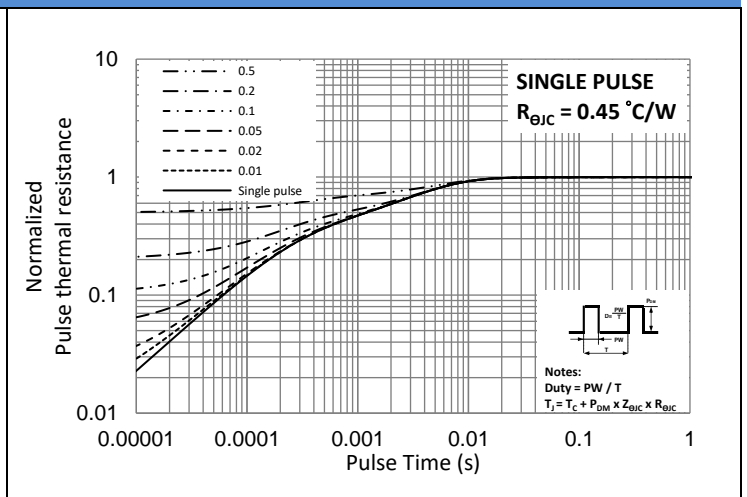
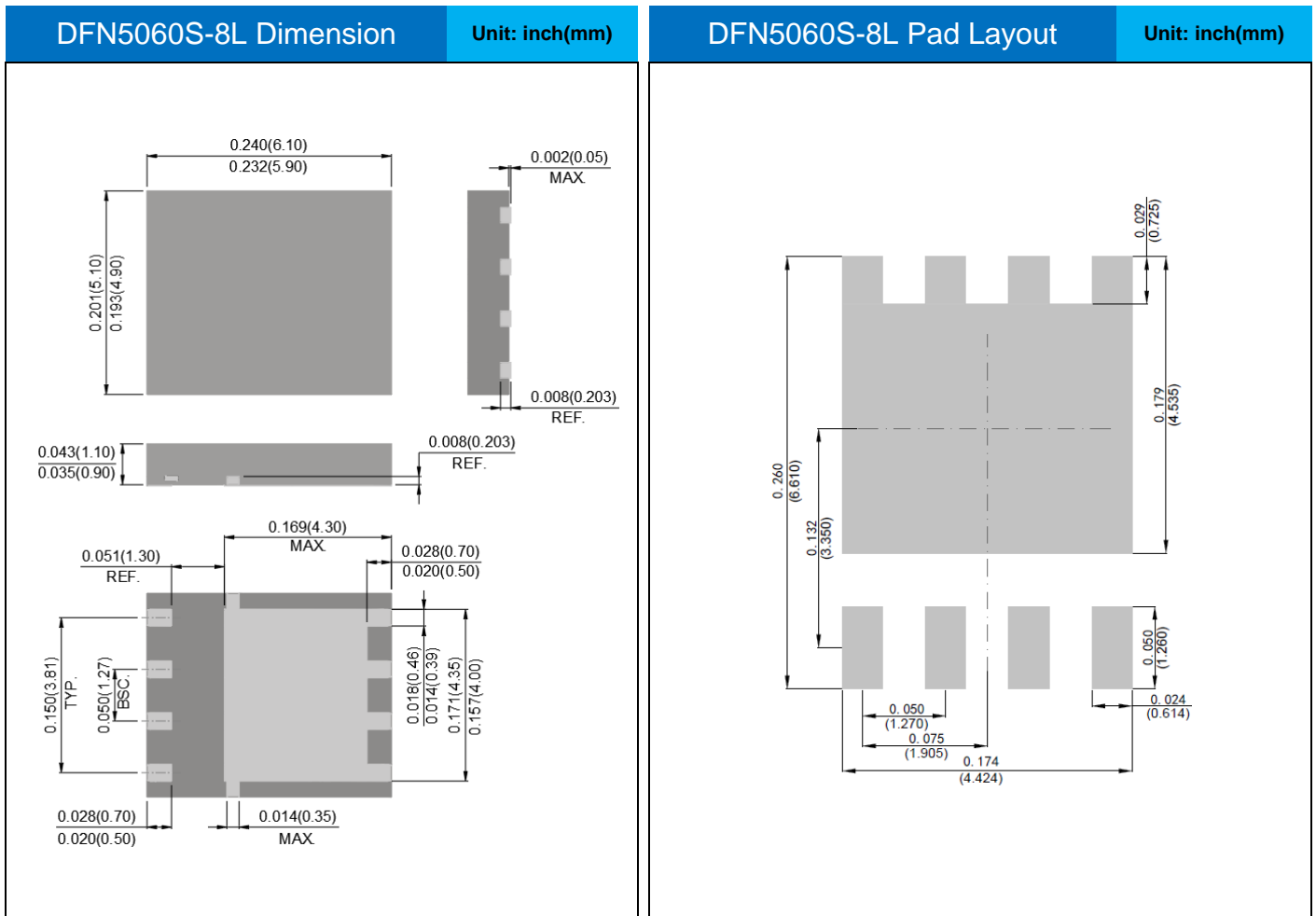


Fig.12 Normalized Transient Thermal Impedance

Product and Packing Information

Part No.	Package Type	Packing Type	Marking
PSMQF020N08NS2	DFN5060S-8L	3000pcs / 13" reel	020N08NS

Packaging Information & Mounting Pad Layout



Marking Diagram

PJ	Y = Year Code
020N08NS	W = Week Code (A~Z)
YWLL x	LL = Lot Code (00~99)
	x = Production Line Code

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