



# PE13SD03M4Q

## Ultra Low Capacitance ESD PROTECTION

**Voltage**

**3.3 V**

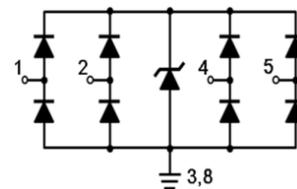
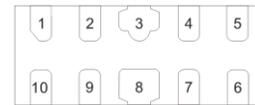
### Features

- IEC61000-4-2(ESD) :  $\pm 15\text{kV}$  Air,  $\pm 14\text{kV}$  Contact
- IEC61000-4-4(EFT) : 40A(5/50ns)
- IEC61000-4-5(Lightning) : 6A(8/20 $\mu\text{s}$ )
- Low leakage current, maximum of 1 $\mu\text{A}$  at rated voltage
- Ultra low clamping voltage
- Lead free in compliance with EU RoHS 2.0
- Green molding compound as per IEC 61249 standard

### Mechanical Data

- Case : DFN2510A-10L Package
- Terminals : Solderable per MIL-STD-750, Method 2026
- Approx. Weight : 0.003 grams

DFN2510A-10L



## Maximum Ratings and Thermal Characteristics (T<sub>A</sub> = 25°C unless otherwise noted)

PARAMETER	SYMBOL	LIMIT	UNITS
ESD IEC61000-4-2(Air)	V <sub>ESD</sub>	$\pm 15$	kV
ESD IEC61000-4-2(Contact)		$\pm 14$	
Operating Junction Temperature Range	T <sub>J</sub>	-55~85	°C
Storage Temperature Range	T <sub>STG</sub>	-55~150	°C



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## Electrical Characteristics (T<sub>A</sub> = 25°C unless otherwise noted)

PARAMETER	SYMBOL	TEST CONDITION	MIN.	TYP.	MAX.	UNITS
Reverse Stand-Off Voltage <sup>(Note 1)</sup>	V <sub>RWM</sub>	-	-	-	3.3	V
Reverse Breakdown Voltage	V <sub>BR</sub>	I <sub>BR</sub> = 1 mA	5.5	-	16	V
Forward Voltage	V <sub>F</sub>	I <sub>F</sub> = 15mA, I/O Pin to GND	-	1	-	V
Reverse Leakage Current	I <sub>R</sub>	V <sub>R</sub> = 3.3 V, I/O Pin to GND	-	-	1	μA
Clamping Voltage	V <sub>CL</sub>	I <sub>PP</sub> = 5 A, t <sub>P</sub> = 8/20 μs, I/O Pin to GND	-	3.3	-	V
Clamping Voltage TLP <sup>(Note 2)</sup>	V <sub>CL</sub>	I <sub>PP</sub> = 8 A, t <sub>P</sub> = 100 ns, I/O Pin to GND	-	3.9	-	V
		I <sub>PP</sub> = 16 A, t <sub>P</sub> = 100 ns, I/O Pin to GND	-	5.5	-	
Dynamic Resistance	R <sub>DYN</sub>	t <sub>P</sub> = 100 ns	-	0.2	-	Ω
Off State Junction Capacitance <sup>(Note 3)</sup>	C <sub>J</sub>	1.65Vdc Bias, f = 1 MHz, I/O Pins to GND	-	0.27	0.32	pF
		1.65Vdc Bias, f = 1 MHz, Between I/O Pins	-	0.05	0.1	

**NOTES :**

1. A transient suppressor is selected according to the working peak reverse voltage(V<sub>RWM</sub>), which should be equal to or greater than the DC or continuous peak operation voltage level.
2. Testing using Transmission Line Pulse (TLP) conditions: Z<sub>0</sub> = 50 Ω, t<sub>P</sub> = 100 ns.
3. This parameter is guaranteed by design.
4. This snap-back behavior strongly reduces the clamping voltage to the system behind the ESD protection during an ESD event. Do not connect unlimited DC current sources to the data lines to avoid the ESD protection device maintain in snap-back state after exceeding breakdown voltage



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## TYPICAL CHARACTERISTIC CURVES

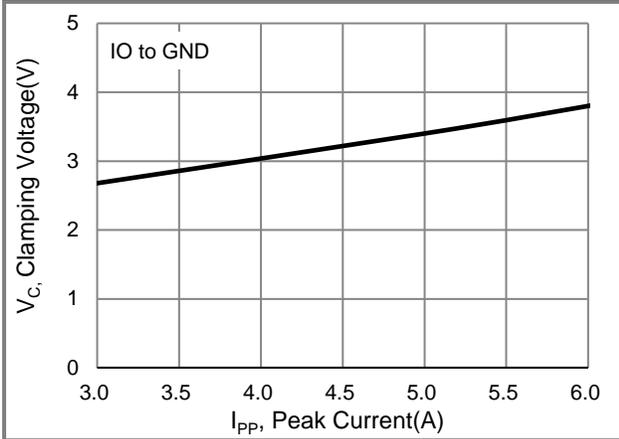


Fig.1 Typical Peak Clamping Voltage

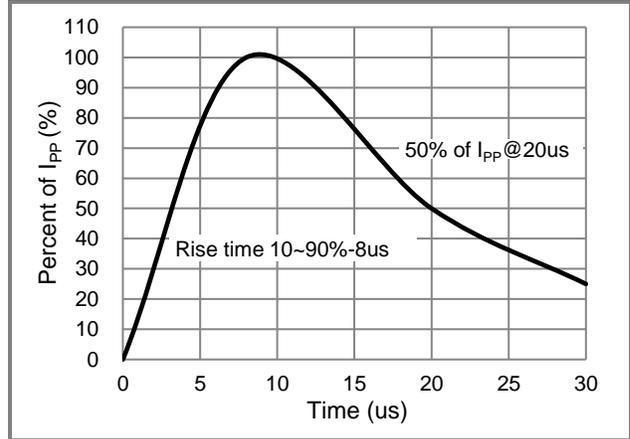


Fig.2 Pulse Waveform

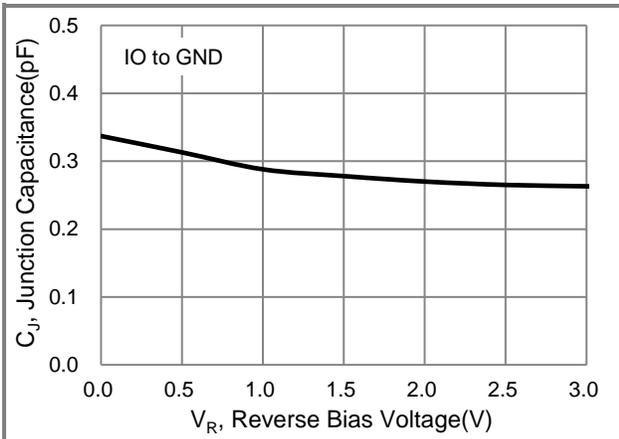


Fig.3 Typical Junction Capacitance

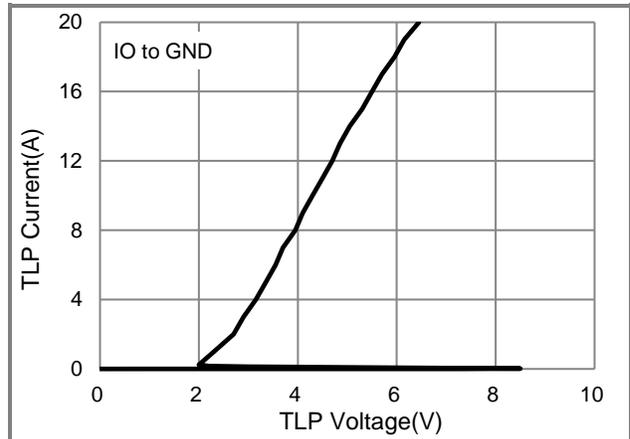


Fig.4 TLP Measurement

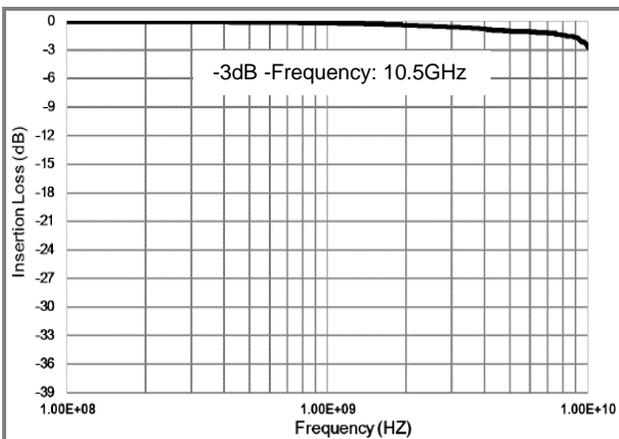


Fig.5 Insertion Loss

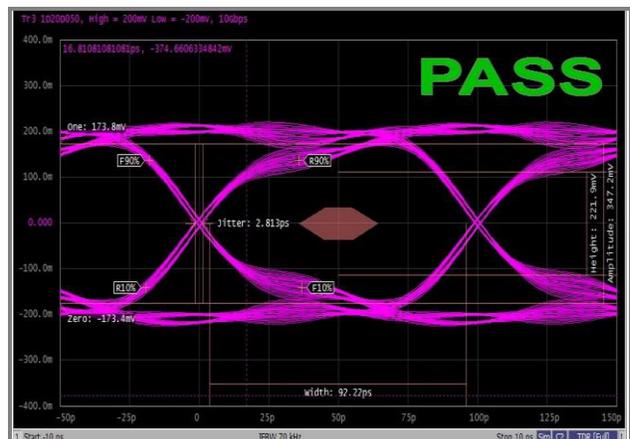


Fig.6 10Gb/s USB3.2 Gen2x1 Eye Diagram

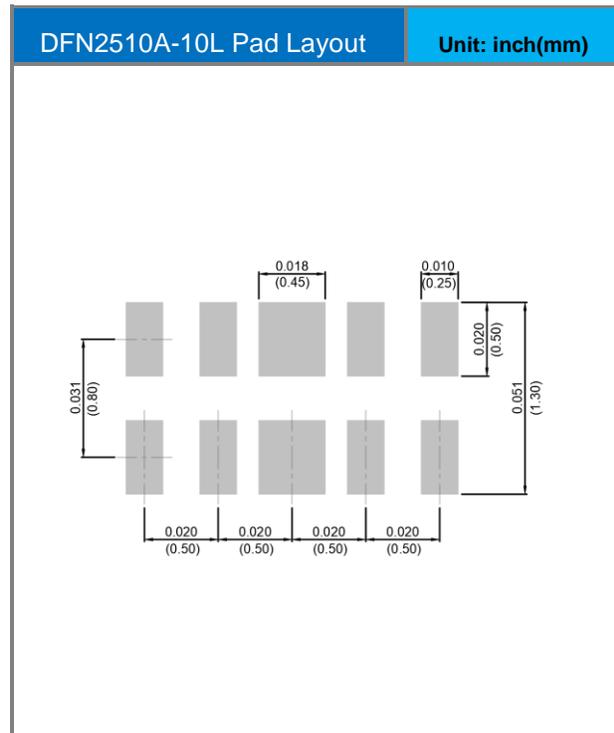
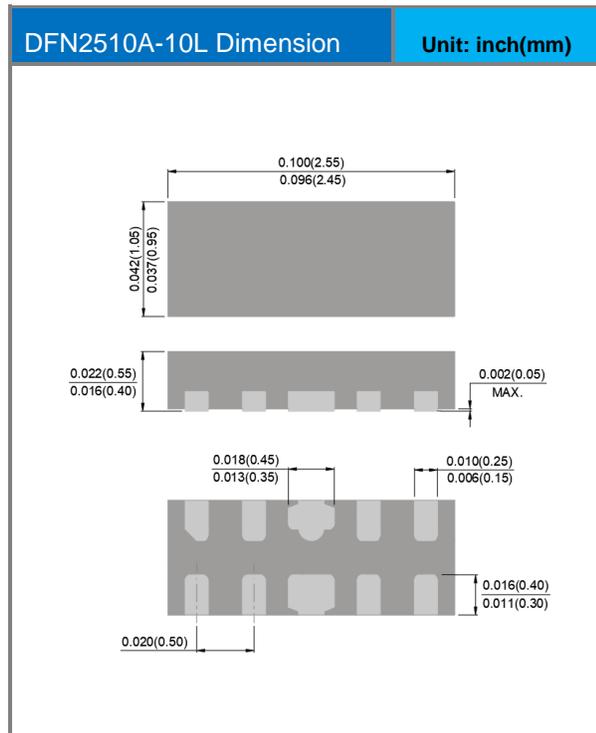


# PE13SD03M4Q

Part No. Packing Code Version

Part No.	Package Type	Packing Type	Marking	Version
PE13SD03M4Q	DFN2510A-10L	3K pcs / 7" reel	3D3	Halogen free RoHS compliant

## Packaging Information & Mounting Pad Layout





## PE13SD03M4Q

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