AN-PJ1003

Understanding PANJIT Medium Voltage and Super Junction MOSFET Datasheet Parameters

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1 Revision History

Rev.	Revision Description	Edit by	Date
Rev.00	Document Release	Arief Noor Rahman	2022/07/14
Rev.01	Products Lineup	Shane Yang	2022/08/26

2 Introduction

Power MOSFETs are widely used as switches in various high efficiency power converter applications for its low switching and conduction losses. During design process, engineers use device datasheet provided by manufacturer to understand the device characteristic and make decision of the device suitability for the circuit. Despite of the crucial role of a datasheet, engineers often have misconceptions on datasheet parameters. This application note is aimed to help engineers to understand datasheet parameters, how they were obtained, and how to correlate it to circuit performance.

In PANJIT, we have developed MOSFET technologies for medium voltage (MV-MOSFET) range (60V, 80V, and 100V) and super junction (SJ-MOSFET) range (600V and 650V). In the next sections, we present our MV-MOSFET and SJ-MOSFET lineup followed with the explanation on datasheet parameters and how they were obtained. For some specific parameters with big discrepancy between MV- and SJ-MOSFETs, further explanation is provided.

3 PANJIT Medium Voltage MOSFET structure and lineup

In PANJIT, the MV-MOSFET lineup has been developed using shielded gate trench (SGT) structure as shown in Figure 1. The shield is internally connected to source pin which protecting the gate finger from the drain by reducing the gate to drain capacitance and increasing drain to source capacitance. Resulting in improved gate robustness and lower possibility of false turn-on. Furthermore, the shield is created using polysilicon which have significantly higher resistance than metal that forms a series RC connection between drain to source which behaves as an internal snubber. Where it benefits the device with softer switching characteristic and lower EMI emission. Our current MV-MOSFET lineup is provided in Table 1.

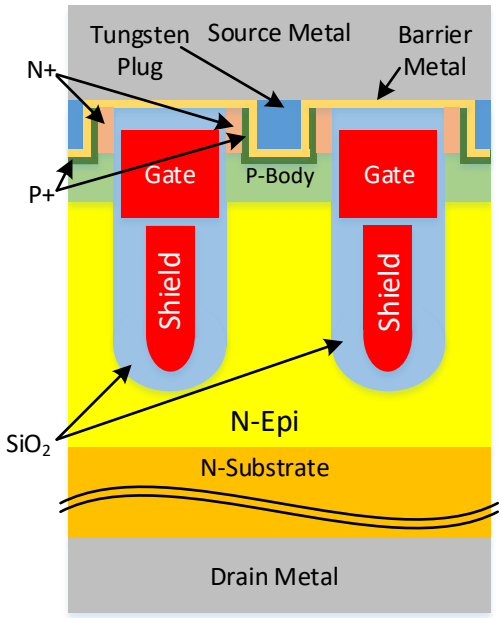

Figure 1. PANJIT MV-MOSFET with shielded gate trench structure

Table 1. PANJIT 100V MV-MOSFET lineup

*in development

Voltage (V)	SL/ LL	TO-LL	TO-263	DFN5060-8L	DFN5060S-8L	DFN3333S-8L	TO-220AB-L
							
100	SL	***PSMN015N10NS2** (1.5mohm)	***PSMB033N10NS2** (3.3mohm)	**PSMQC040N10NS2** (4.4mohm)	***PSMQF026N10NS2** (2.6mohm)	***PSMQE085N10NS2** (8.5mohm)	***PSMP033N10NS2** (3.3mohm)
100	SL	***PSMN027N10NS2** (2.7mohm)	***PSMB042N10NS2** (4.2mohm)	***PSMQC072N10NS2** (7.2mohm)	***PSMQF035N10NS2** (3.5mohm)	***PSMQE092N10NS2** (9.2mohm)	***PSMP042N10NS2** (4.2mohm)
100	SL		**PSMB050N10NS2** (5.0mohm)	***PSMQC089N10NS2** (8.9mohm)			**PSMP050N10NS2** (5.0mohm)
100	SL						***PSMP093N10NS2** (9.3mohm)

Voltage (V)	SL/ LL	DFN5060-8L	DFN5060S-8L	DFN3333-8L (Cu Wire)	DFN3333S-8L (Cu Clip)	TO-252AA (DPAK)
						
100	LL	***PSMQC038N10LS2** (3.8mohm)	***PSMQF025N10LS2** (2.5mohm)	***PSMQB230N10LS2** (23mohm)	***PSMQE080N10LS2** (8.0mohm)	***PSMD081N10LS2** (8.1mohm)
100	LL	***PSMQC055N10LS2** (5.5mohm)	***PSMQF034N10LS2** (3.4mohm)			***PSMD093N10LS2** (9.3mohm)
100	LL	***PSMQC078N10LS2** (7.8mohm)				***PSMD130N10LS2** (13mohm)
100	LL	***PSMQC090N10LS2** (9mohm)				***PSMD240N10LS2** (24mohm)
100	LL	***PSMQC120N10LS2** (12mohm)				
100	LL	***PSMQC240N10LS2** (24mohm)				

4 PANJIT Super Junction MOSFET structure and lineup

The main design objective for SJ-MOSFET is to achieve low ON resistance and low parasitic capacitance to reduce both conduction and switching losses. The solution is to use a deep-trench structure also known as super-junction structure that is created using P-pillar trench. Figure 2 shows the structure of PANJIT super-junction MOSFET (SJ-MOSFET). Compared to the predecessor design (planar structure), super-junction structure is able to achieve a uniform electric field throughout the epitaxial layers as depicted in Figure 2 (right). Where it allows for higher doping concentration and thinner epitaxial layer. Both, resulting in significantly lower specific ON resistance which allows for smaller die size and consequently lower parasitic capacitance compared to its predecessor. Our current SJ-MOSFET lineup offering 600V-650V voltage rating is presented in Table 2.

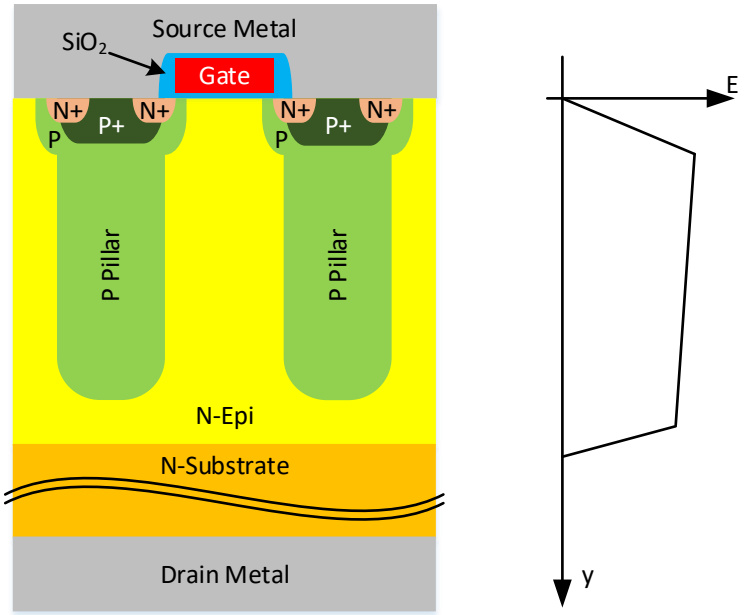

Figure 2. PANJIT HV-MOSFET with super-junction structure

Table 2. PANJIT SJ-MOSFET lineup

Series	BV (V)	Rdson (mohm)	TO-247	ITO-220AB-F	TO-220AB-L	TO-252AA	TO-263
SJ MOSFET 600V	600	74	PJMH074N60FRC				
		99	PJMH099N60EC				
		120	PJMH120N60EC	PJMF120N60EC	PJMP120N60EC		
		190	PJMH190N60E1	PJMF190N60E1	PJMP190N60E1		
		280		PJMF280N60E1			
		360		PJMF360N60EC	PJMP360N60EC	PJMD360N60EC	
		580		PJMF580N60E1		PJMD580N60E1	
		900		PJMF900N60EC	PJMP900N60EC	PJMD900N60EC	
SJ MOSFET 650V	650	130		PJMF130N65EC	PJMP130N65EC		PJMB130N65EC
		210		PJMF210N65EC	PJMP210N65EC		PJMB210N65EC
		280		PJMF280N65E1			
		310		PJMF310N65EC	PJMP310N65EC		PJMB310N65EC
		390		PJMF390N65EC	PJMP390N65EC	PJMD390N65EC	PJMB390N65EC
		600		PJMF600N65E1		PJMD600N65E1	
		990		PJMF990N65EC	PJMP990N65EC	PJMD990N65EC	

5 Understanding MOSFET Datasheet Parameters

Datasheet provides information to the engineers about various device parameters and some additional information. However, many of the information are not exactly relevant for switching converter application while some are not very straight-forward to understand. The definition of each parameters and the measurement circuit and method are presented to help the reader to thoroughly understand every parameter.

As an example, our PANJIT PJMF390N65EC (650V, 10A, 390 mΩ) [1] super-junction high voltage MOSFET is used in this explanation. The explanation of each parameters is explained in the next sub-sections.

5.1 Highlighted feature and introduction

This section shows the highlighted feature of the device, typically the basic such as part number, voltage and current ratings, and resistance rating. Highlighted feature of the device such as a few test items and device compliance are also commonly mentioned in this section. Lastly, the intended market/application and sometimes intended circuit topology are also typically mentioned to help the customer to choose the device.

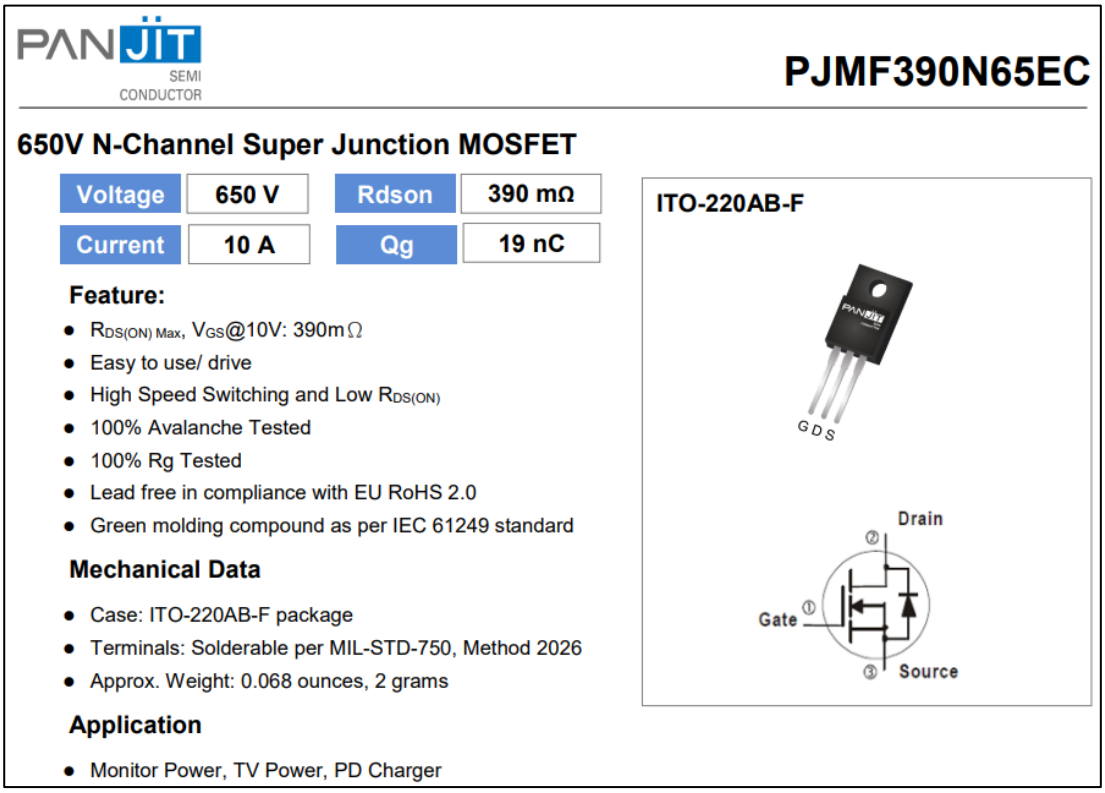

Figure 2. Datasheet of PJMF390N65EC, highlighted feature and introduction

In PANJIT MOSFET datasheet, we mentioned 100% avalanche tested and 100% R_g (internal gate resistance) tested on top of the typical test to give more confidence to the engineer about our device reliability/ruggedness performance. The avalanche performance is tested at the manufacturing site for every production device at 50% rated avalanche energy. The R_g is tested as an indicator of the semiconductor process manufacturing quality (epitaxial, etching, deposition, doping, oxide growing, etc.) and compared with a set toleration limit. Devices that failed on either or both test are screened out from the final product as it is indicated to have defects and will fail prematurely if otherwise assembled into the customer product.

The MOSFET is targeted for market monitor power, TV power and PD charger, which practically is based on ZVS topologies such as LLC or active clamp flyback, and also PFC for application

greater than 75W.

5.2 Absolute maximum rating

Table 3 provides the absolute operating limits of the device and the circuit should be designed to operate the device within the limits for reliable operation. It is important to maintain a reasonable operating margin from the absolute maximum rating to ensure the limits are never violated while operating too close to the maximum rating can resulting in shortened expected lifetime.

Table 3. Absolute maximum ratings of PJMF390N65EC

PARAMETER		SYMBOL	LIMIT	UNITS
Drain-Source Voltage @ $T_{j,max}$		V_{DS}	700	V
Drain-Source Voltage		V_{DS}	650	
Gate-Source Voltage		V_{GS}	±30	
Continuous Drain Current	Tc = 25°C	I_D	10	A
	Tc = 100°C		6.2	
Pulsed Drain Current	Tc = 25°C	I_{DM}	22	A
Single Pulse Avalanche Energy		E_{AS}	220	mJ
MOSFET dv/dt ruggedness		dV/dt	50	V/ns
Power Dissipation	Tc = 25°C	P_D	29.5	W
	Tc = 100°C		12	
Insulation Withstand Voltage for ITO-220AB-F		V_{ISO}	3.5	kV
Operating Junction and Storage Temperature Range		T_J, T_{STG}	-55 ~ 150	°C

V_{DS} and V_{DS} (@$T_{j,max}$) : the voltage limit that may be applied before the drain source leakage current (I_{dss}) exceed a limit threshold (100μA – 1mA) which resulting in excessive loss. For converter design, it is highly recommended to make sure to keep a reasonable margin for the V_{ds} spike to this absolute limit.

V_{GS} : voltage is the allowable voltage limit on the gate. The gate structure of a MOSFET is only separated with a very thin oxide (SiO_2) layer that is prone to failure if excessive voltage is applied.I_D : Rated drain current is the required drain to source continuous current (pure continuous conduction loss) to increase the T_j to maximum T_j when the device is placed on a “infinite heatsink”. Infinite heatsink is a heatsink with tightly controlled temperature which is maintained at fixed temperature (25°C and 100°C). It is common for the manufacturer to use theoretical calculation as shown in Equation 1 to obtain this parameter instead of actual measurement result. Specific case for low voltage and medium voltage MOSFET that has >100A current rating, the drain current rating often specified for the MOSFET die capability and the bond wire limit.

$$I_D = \sqrt{\frac{T_{j,max} - T_c}{R_{ds}(T_{j,max}) \ . R_{th,jc}}} \quad (1)$$

I_{DM} : Peak drain current is the maximum allowable short current pulse. When the device is exposed to high current on a short pulse time (Typ. ≤1ms) the device thermal characteristic is considered to be adiabatic. Where all the power dissipation is used to increase the junction temperature with no heat energy flow out to heatsink or surrounding space. This parameter is also commonly calculated theoretically by solving Equation 2 with C_{th} defined as MOSFET assembly heat capacity. For some manufacturers, I_{DM} is defined as a fixed multiply of rated I_D (Typ. 3x to 4x). Furthermore, another factor such as bond wire limit or drain current cutoff may limit the I_{DM} capability.

$$C_{th}.\left(T_{j,max} - 25°C\right) = \int_0^t {I_{DM}}^2 . R_{ds}(T_j) \ dt \quad (2)$$

E_{AS} : Maximum allowable single pulse avalanche energy is the maximum energy that can be . Under avalanche, the MOSFET is exposed to V_{DS} = BV_{DSS} and high Id simultaneously which resulting in very high power dissipation and fast internal temperature rise. This process occurred in <100μs thus considered to be adiabatic system. Similar to I_{DM}, this parameter is also strongly related to the device heat capacity. This parameter is obtained using unclamped inductive circuit test as shown in Figure 3.

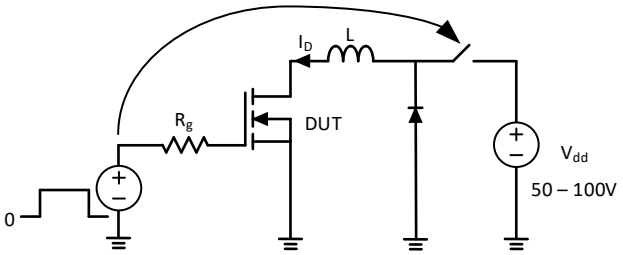

Figure 3. Measurement circuit for E_{AS} characterization

$$E_{AS} = \frac{L.{I_D}^2}{2} \quad (3)$$

dV/dt : Maximum V_{DS} slew rate dV_{DS}/dt transient during device turn off switching. A MOSFET exhibit internal RC-npn parasitic structure as shown in Figure 4. When the device is operated with dV_{DS}/dt above the limit, the leakage C_b current will be enough to turn on the npn. Where the npn will be latched ON and causing destructive failure. This phenomenon is more severe on SJ- than on MV- MOSFET due to the higher dV/dt, and used to be a major reliability concern on SJ-MOSFET.

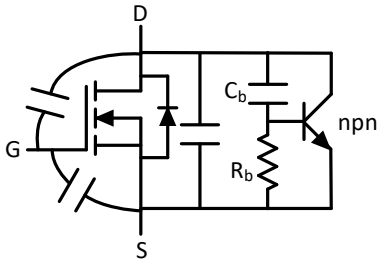

Figure 4. MOSFET internal parasitic npn structure

P_D : is the maximum power dissipation is the required MOSFET power dissipation to increase T_j to $T_{j,max}$ with the device attached to infinite heatsink with specified fixed temperature. This parameter often calculated using Equation 4.

$$P_D = \frac{T_{j,max} - T_c}{R_{th,jc}} \quad (4)$$

V_{ISO} : is the insulating withstanding voltage is the guaranteed package isolation voltage limit based on AC 60Hz test for 1 minutes test duration. This information is only available for MOSFET with isolated TO package.

5.3 Thermal and electrical characteristics

This section provides information regarding the thermal and electrical parameters for a specific test condition. Information presented in this sections is meant to provide some idea on the device characteristic/performance but not on the exact device behavior.

Table 4. Thermal resistance characteristics of PJMF390N65EC

PARAMETER		SYMBOL	LIMIT	UNITS
Thermal Resistance	Junction-to-Case	$R_{\theta,jc}$	4.2	°C/W
	Junction-to-Ambient	$R_{\theta,ja}$	62.5	

For thermal resistance, two parameters are provided junction-to-case and junction-to-ambient thermal resistance. On the typical application where the MOSFET is attached to a heatsink, R θ, jc is used to described the thermal resistance between the junction to the back-side surface of the MOSFET. Together $R_{\theta,JC}$, $R_{\theta,TIM}$, and $R_{\theta,HS\text{-}Ambient}$ are then combined together to form equivalent thermal circuit as shown in Figure 5 which can be used to model or estimate the junction temperature. When the MOSFET is not attached to a heatsink, $R_{\theta,JA}$ is used for junction temperature estimation.

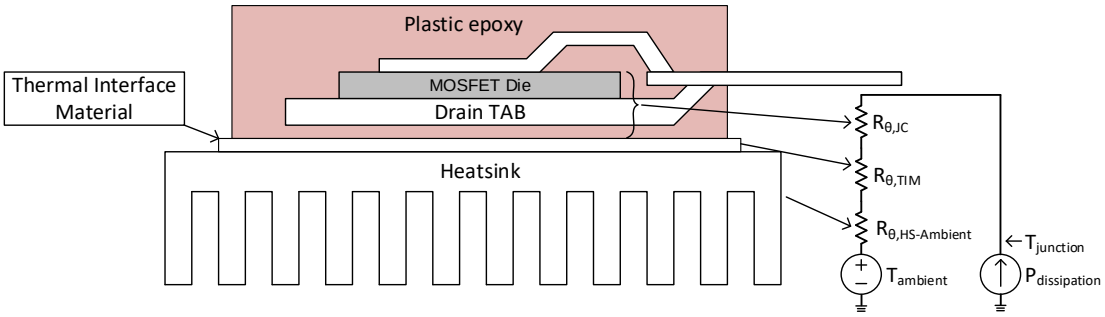

Figure 5. MOSFET thermal stackup with heatsink attached

The electrical parameters of the MOSFET are typically categorized into three groups. First, static parameters provide information regarding device characteristics with all V_{DS}, I_D, and V_{GS} are constant during the test. Second, dynamic parameters provide information regarding device characteristics during switching transition. Third, body diode parameters, provide the information on the forward voltage and reverse recovery characteristics of the device. Those three parameters were obtained at T_j = 25°C unless stated otherwise.

Table 5. Static electrical characteristics of PJMF390N65EC

PARAMETER	SYMBOL	TEST CONDITION	MIN.	TYP.	MAX	UNITS
Static						
Drain-Source Breakdown Voltage	BV_{DSS}	V_{GS}=0V, I_D=250uA	650	730	-	V
Gate Threshold Voltage	$V_{GS(th)}$	V_{DS}=V_{GS}, I_D=250uA	2	3	4	
Drain-Source On-State Resistance	$R_{DS(on)}$	V_{GS}=10V, I_D=5.0A	-	340	390	mΩ
Zero Gate Voltage Drain Current	I_{DSS}	V_{DS}=650V, V_{GS}=0V	-	-	1	uA
Gate-Source Leakage Current	I_{GSS}	V_{GS}=±30V, V_{DS}=0V	-	-	±100	nA
Transfer Characteristics	gfs	V_{DS}=20V, I_D=11A	-	10	-	S

BV_{DSS} : is the measured V_{DS} when the leakage current reaching to a specified threshold (250μA – 1mA) with gate shorted to source.

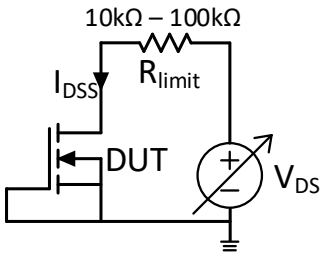

Figure 6. BV_{DSS} and I_{DSS} measurement circuit

$V_{GS(th)}$: is the measured gate voltage when the current starts to flow from drain to source. This parameter is measured shorting the drain and gate pin then applying a small current (250μA – 1mA) from drain pin to source pin.

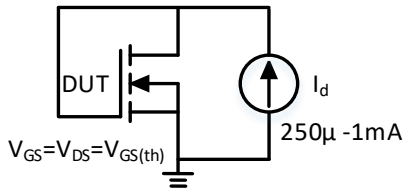

Figure 7. Gate threshold voltage measurement circuit

$R_{DS(on)}$: is the measured drain to source resistance at the specified gate-source bias voltage and drain-source current. The specified drain-source current is only applied to the DUT for a very short duration (100 μs – 500 μs) to limit the self-heating effect raise the T_j during the measurement duration.

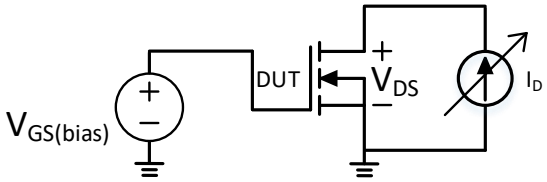

Figure 8. ON resistance measurement circuit

I_{DSS} : is the measured drain to source leakage current at the specified rated device V_{DS} voltage. This parameter is obtained using the circuit shown in Figure 6 with V_{DS} is set at the voltage device rating.

I_{GSS} : is the measured gate leakage current at the specified maximum positive and negative gate voltage bias.

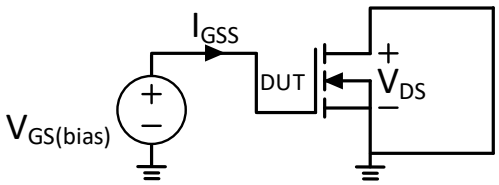

Figure 9. Gate leakage current measurement circuit

gfs : is the MOSFET transconductance which is defined as the slope/ratio between V_{GS}/I_D at the specified I_D with the MOSFET drain-source biased with a constant voltage. The gfs is also shown in the V_{GS} - I_D curve (Section 5.4, Figure 18(b)).

Table 6. Dynamic electrical characteristics of PJMF390N65EC

PARAMETER	SYMBOL	TEST CONDITION	MIN.	TYP.	MAX	UNITS
Dynamic						
Total Gate Charge	Q_g	V_{DS}=520V, I_D=11A, V_{GS}=10V	-	19	-	nC
Gate-Source Charge	Q_{gs}		-	4	-	
Gate-Drain Charge	Q_{gd}		-	8	-	

Input Capacitance	C_{iss}	V_{DS}=400V, V_{GS}=0V, f=250kHz	-	726	-	pF
Output Capacitance	C_{oss}		-	29	-	
Reverse Transfer Capacitance	C_{rss}		-	8	-	
Effective Output Capacitance Energy Related	$C_{O(er)}$	V_{DS}=0V to 400V, V_{GS}=0V, f=250kHz	-	37	-	
Turn-On Delay Time	$t_{d(on)}$	V_{DD}=325V, I_D=11A, V_{GS}=10V,R_g=25Ω	-	30	-	ns
Turn-On Rise Time	$t_{r(on)}$		-	50	-	
Turn-Off Delay Time	$t_{d(off)}$		-	87	-	
Turn-Off Fall Time	t_f		-	42	-	
Gate Resistance	R_g	f=1 MHz	-	6.8	-	Ω

Q_g, Q_{gs}, and Q_{gd}: are the gate charge characteristic of the MOSFET. Q_{gs} is defined as the required charge needed to raise the gate voltage from the OFF-state up to the plateau voltage ($V_{gs,pl}$). The Q_{gd} is is defined as the required charge needed to fully discharge the V_{DS}. The Q_g is defined as the required charge needed to raise the gate voltage from OFF-state to VGS-ON under hard-switching condition. Measurement for gate charge is conducted using the circuit shown in Figure 10 with the specified V_{DD} supply voltage and R_{load} to reach the specified ON current. The gate charge of the DUT is measured by charging the gate/turning on the MOSFET with very low current source (< 5mA) or using totem-pole gate driver with large gate resistance.

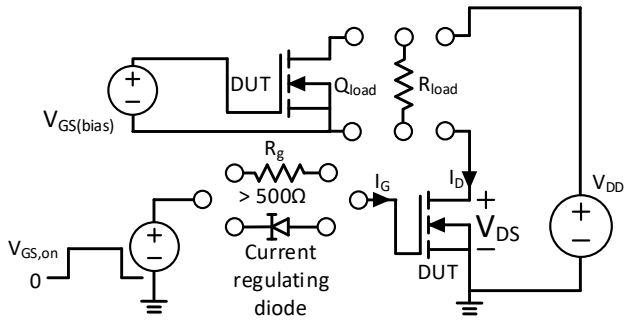

Figure 10. Gate charge measurement circuit

$$Q_g = \int_0^t I_G \, dt \quad (5)$$

Ciss, Coss, and Crss : are the input, output, and reverse parasitic capacitance of the MOSFFET as described by Figure 11. The MOSFET parasitic capacitance is highly nonlinear since the capacitance is formed by non-linear depletion region which is related to the applied reverse bias voltage. Figure 12 shows the measurement circuit used to obtained the parasitic capacitance and also applying V_{DS} bias voltage.

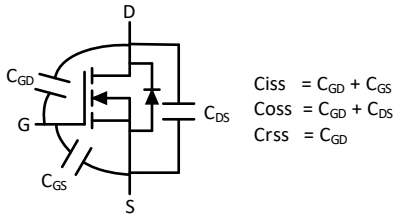

Figure 11. Correlation of different parasitic capacitances

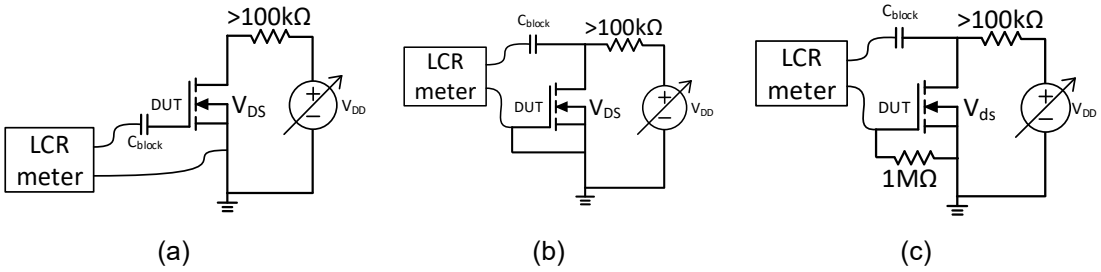

Figure 12. Parasitic capacitance measurement circuit: (a) Ciss, (b) Coss, and (c) Crss

$C_{O(er)}$ and $C_{O(tr)}$: First is the effective output capacitance – energy related which is equivalent linear capacitor value that holds same amount of energy as the MOSFET DUT at a specific V_{DS} voltage. Second is the effective output capacitance – time related which is the equivalent linear capacitor value that holds the same amount of charge as the MOSFET DUT at a specific V_{DS} voltage. The $C_{O(er)}$ is related to capacitive energy loss especially during hard-switching operation. The $C_{O(tr)}$ is related to the time required to discharge the output capacitance, mostly used for calculating the required dead-time in ZVS converter. Both parameters can be obtained by using a series RC circuit with the C formed by MOSFET Coss, as depicted in Figure 13, then Equations 6 and 7 is used to calculate the parameters result. Meanwhile, Equations 8 and 9 are used by some device manufacturers to calculate the $C_{O(er)}$ and $C_{O(tr)}$ from Coss measurement curves as depicted in Figure 20.

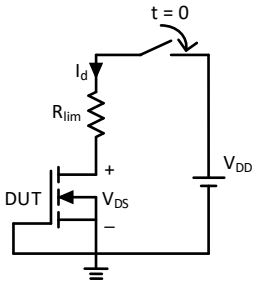

Figure 13. $C_{O(er)}$ and $C_{O(tr)}$ experimental measurement circuit

$$C_{O(er)}(V) = \frac{2}{V^2}\int_0^{t(V)} V_{DS}.I_D \quad dt \tag{6}$$

$$C_{O(tr)}(V) = \frac{1}{t(V).R_{lim}} \ln\left(1 - \frac{V}{V_{DD}}\right) \tag{7}$$

$$C_{O(er)}(V) = \frac{2}{V^2}\int_0^{t(V)} C_{OSS}(V).V \quad dV \tag{8}$$

$$C_{O(tr)}(V) = \frac{Q_{OSS}(V)}{V} = \frac{1}{V}\int_0^{V} C_{OSS}(V) \quad dV \tag{9}$$

td(on), tr, td(off), and tf : are the delay and transient time during turn on and turn off switching test with specific R_{load}, V_{DD}, and R_g, and $V_{GS,on}$. The test circuit and measurement definition of these parameters are shown in Figure 14.

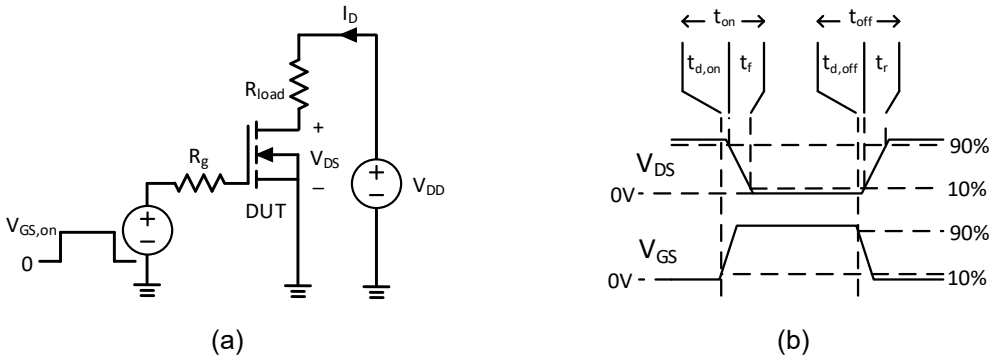

Figure 14. Switching delay and transient, (a) measurement circuit and (b) waveform definition

R_g : is the measured equivalent series resistance of the MOSFET obtained using LCR meter. The measurement circuit is shown in Figure 15 and the R_g is measured at the specified frequency and V_{GS} bias (Typically V_{GS} = 0V if not specified).

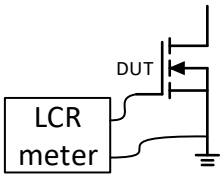

Figure 15. Internal gate resistance measurement

Table 7. Body diode characteristics of PJMF390N65EC

PARAMETER	SYMBOL	TEST CONDITION	MIN.	TYP.	MAX	UNITS
Drain-Source Diode						
Maximum Continuous Drain-Source Diode Forward Current	I_S	-	-	-	10	A
Diode Forward Voltage	V_{SD}	I_S = 10A, V_{GS} = 0V	-	0.89	1.5	V
Reverse Recovery Charge	Q_{rr}	I_S = 11A, dI/dt = 100A/μs	-	3.3	-	μC
Reverse Recovery Time	T_{rr}		-	291	-	ns

I_S : The maximum continuous diode forward current typically is specified at the same device current rating.

V_{SD} : is the forward voltage of the MOSFET body diode measured at the specified forward current. Typical range for V_{SD} is 0.6 to 1 V.

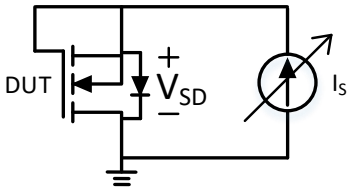

Figure 16. Body diode forward voltage measurement circuit

Q_{rr} and T_{rr} : are the reverse recovery charge and time during hard commutation at the specified diode turn off current slew rate (dI/dt). Slew rate is defined between 50% of forward conduction current and 50% of I_{rrm} (maximum reverse recovery current). Figure 17 shows the measurement circuit for reverse-recovery characteristics and the expected ideal waveform. This parameter is very important when the application requires body diode commutation (e.g. synchronous buck or motor inverter) as well as ZVS converter when body diode commutation may occur when the converter operates at light load or experiencing large transient. The reverse-recovery characteristic of MV and SJ MOSFET is differs significantly, and will be discussed further at the section 6.

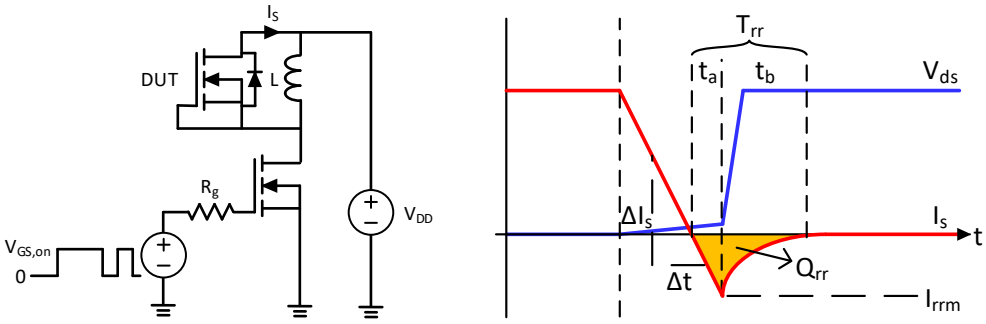

Figure 17. Body diode reverse recovery, (left) measurement circuit and (b) expected ideal waveform.

5.4 Characteristic curves

Further detail of MOSFET characteristics are provided in the form of characteristic curves to provide the correlation between two measurement parameters.

Figure 18 shows the linear characteristic of the MOSFET. First Figure 18(a), V_{DS} - I_D, is measured at specified V_{GS} bias. This curves indicates the MOSFET resistive and cut-off behaviors. Second Figure 18(a), V_{GS} - I_D is measured at the specified V_{DS} bias. This curves may indicate the effectiveness of R_g variation to tune the switching behavior, with steeper curves (higher gfs) resulting in R_g variation to be less effective. Additionally, it may indicate the

MOSFET performance for linear application. Nevertheless, unless the MOSFET is designed/optimized for linear application, typical power MOSFET has small die size and thus has very weak performance in linear application. These linear characteristics are typically not used for switching converter design/applications.

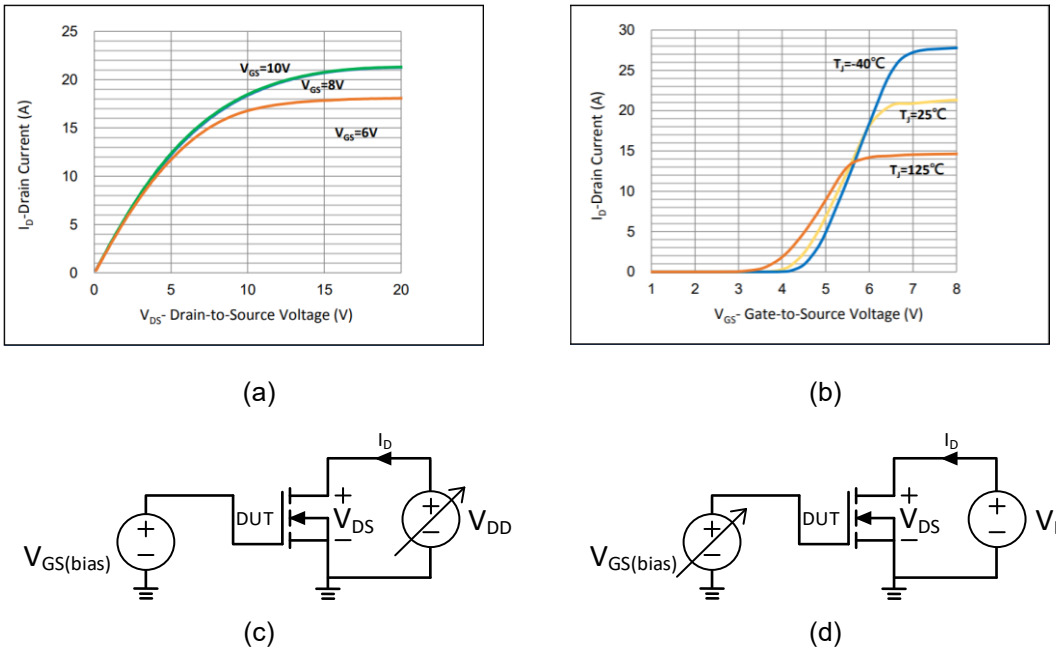

Figure 18. Linear characteristic curves, (a)V_{DS} - I_D and (b)V_{GS} - I_D and its respective measurement circuit (c) and (d)

Figure 19 (a) shows I_D - $R_{DS(on)}$ relationship at fix specified V_{GS} bias. At the large drain current beyond the MOSFET rated current, the MOSFET exhibit cut-off behavior where the resistance increases exponentially. MOSFET resistance also increases proportionally with the junction temperature as depicted in Figure 19(b). Both parameters are measured using circuit shown in Figure 8.

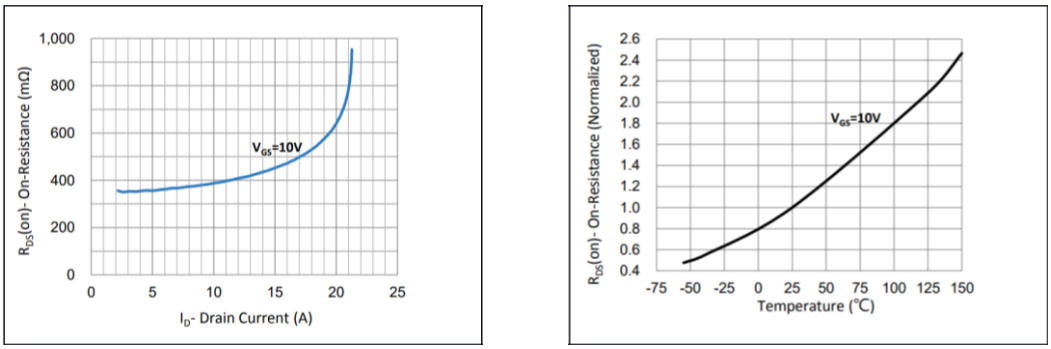

Figure 19. ON resistance characteristic (a)$R_{DS(on)}$ - I_D and (b)Temp – $R_{DS(on)}$

Figure 20 shows the relationship between parasitic capacitances (Ciss, Coss, Crss) to V_{DS} bias. In a MOSFET, as the parasitic capacitance are formed by both physical dielectric (oxide layer) and depletion layer on the pn-junction. Resulting in significant drop in the capacitance at higher voltage especially for Coss and Crss. These capacitances are measured using circuit shown in Figure 12 at the specified excitation frequency.

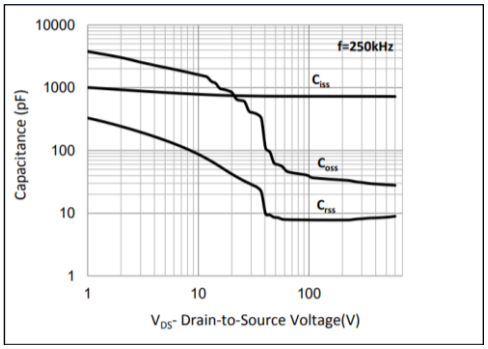

Figure 20. Parasitic capacitance curves to V_{DS} bias characteristic curves

Figure 21 shows the relationship between MOSFET body diode forward current and its forward voltage drop. The body diode has negative temperature coefficient. It is measured using circuit shown in Figure 16.

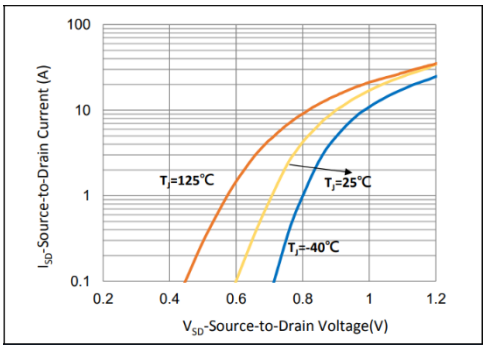

Figure 21. Body diode forward voltage drop, V_{SD} – I_{SD}

Figure 22 shows the gate charge characteristic which is measured using the circuit depicted in Figure 10. Gate plateau voltage is also shown at around 5.3V.

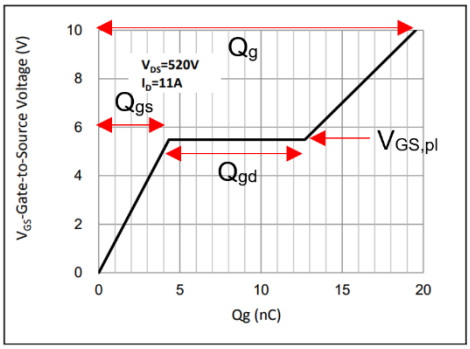

Figure 22. Gate charge characteristic curve

Figure 22 shows the temperature dependent characteristics of the breakdown voltage, gate threshold and continuous current rating. The measurement result was obtained using circuit

provided in Figures 6 and 7 for the first two parameters. The continuous current rating may be obtained using the Equation 1.

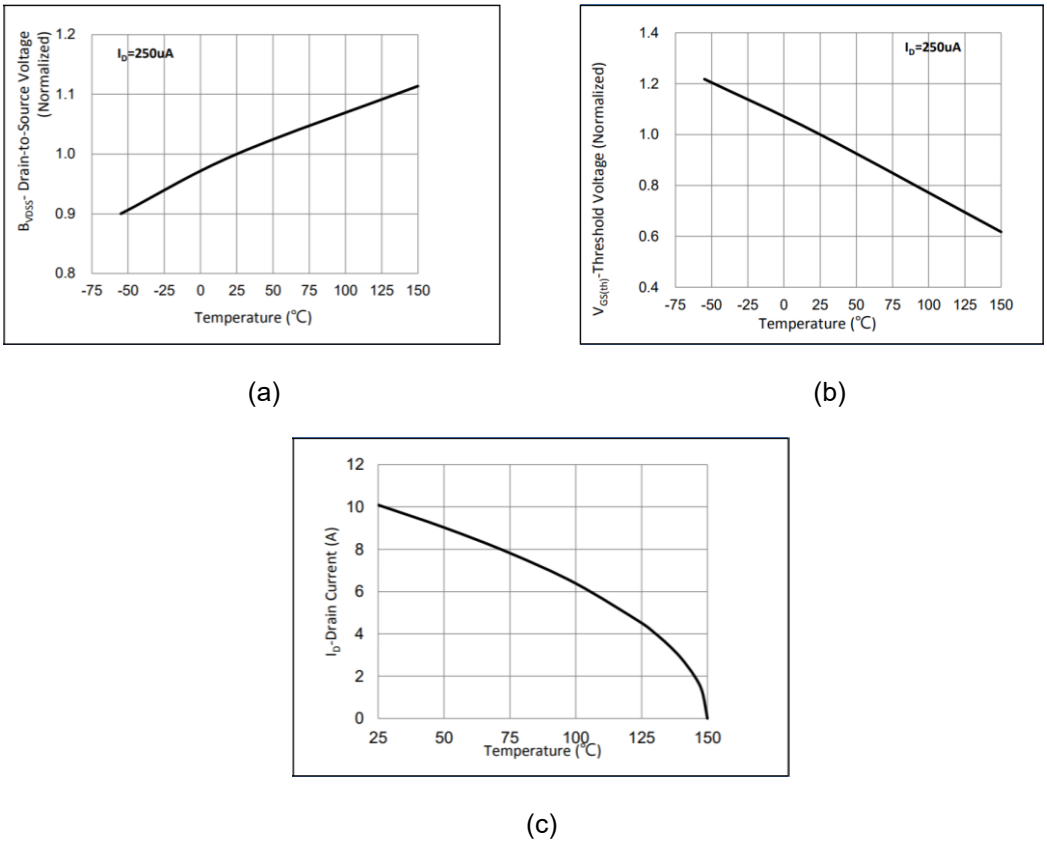

Figure 22. Temperature dependent parameters, (a) breakdown voltage, (b) gate threshold voltage, and (c) continuous current rating

Safe operating area is the safe operating limit of the device that is determined by the current pulse width, (1) resistive limit, (2) pulsed drain current limit, (3) pulse power limit, and (4) break-down voltage limit. SOA is mostly useful for linear application, which is important for linear e-fuse, hot-swap, and load switch applications. Nevertheless, it does not have much use for switching application as the device is exposed to both high voltage and current for <500 ns.

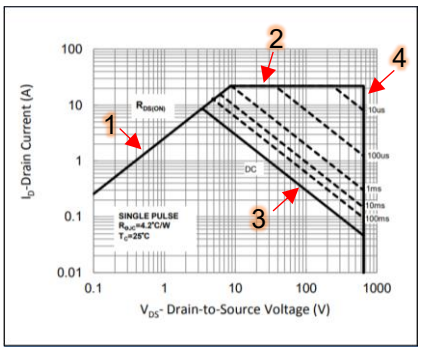

Figure 23. Safe operation area

Normalized transient thermal impedance is measured by applying pulsed power dissipation on

the DUT with varying duty cycle. The resulting characteristic curve is used to create the equivalent RC Cauer or Foster network to create the impedance model of the device.

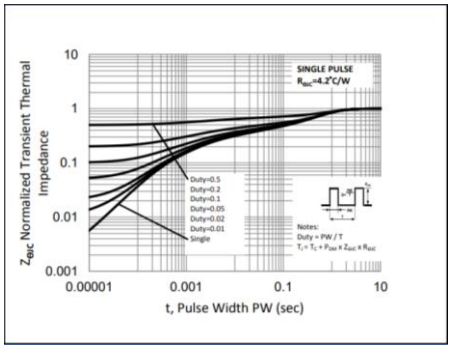

Figure 24. Normalized transient thermal impedance curves

The stored output capacitance energy is shown in Figure 25 for different V_{DS} bias voltage. This curve is used to calculate the total output capacitance loss on a hard switching converter.

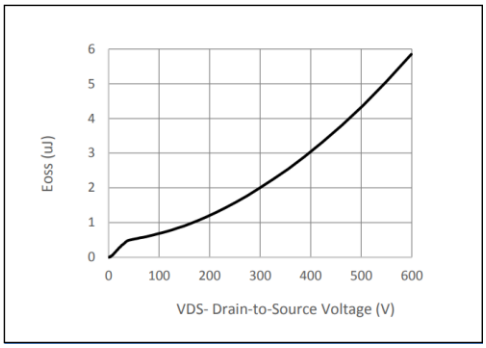

Figure 25. Stored output capacitance energy

5.5 Device characteristic important notice

Structurally, MOSFET with different voltage rating class, such as low, medium, and high voltage are designed with different structure. Where the goal is to optimized the performance based on the switching characteristics, intrinsic capacitances, and ON resistance. For example, low voltage MOSFET tends to have very low ON resistance down to 1mΩ range and used with switching frequency over 500 kHz. In such design the design goal is to minimize the gate charge and minimize the ON resistance. Another example, for high voltage MOSFET, the goal is to achieve high voltage breakdown without sacrificing the ON resistance and also achieving dV/dt ruggedness.

Nevertheless, from the electrical characteristic towards the switching converter operation generally the difference between these MOSFETs are not too significant. Except, body diode reverse recovery performance especially for high voltage super junction MOSFET structure. As mentioned earlier, the super junction is popular for high efficiency switching converter thanks to its low $R_{DS(on)}$. However, the super junction structure has a main downside of creating very large pn-junction for reverse current flow (body diode). Such large pn-junction resulting in large minority carrier (hole) flow during body-diode conduction that needs to recombine during hard commutation. Where, it is resulting in large peak reverse recovery current (I_{rrm}) and “snappy” characteristic of SJ-MOSFET body diode. Figure 26 shows the measured reverse recovery waveform of MV- and

SJ- MOSFETs with current slew-rate during commutation at 980A/μs and 100A/μs respectively. Despite of a ten-times higher the slew-rate, the current waveform of MV-MOSFET has much better reverse recovery behavior: (1) significantly lower I_{rrm}, Q_{rr}, and T_{rr}, (2) better softness factor (t_b/t_a), and (3) clean recovery behavior without oscillation. Meanwhile, the SJ-MOSFET reverse recovery is significantly poorer at all aspect. The oscillation reverse recovery behavior is practically larger on a converter circuit where the slew rate is easily greater than 400 A/μs.

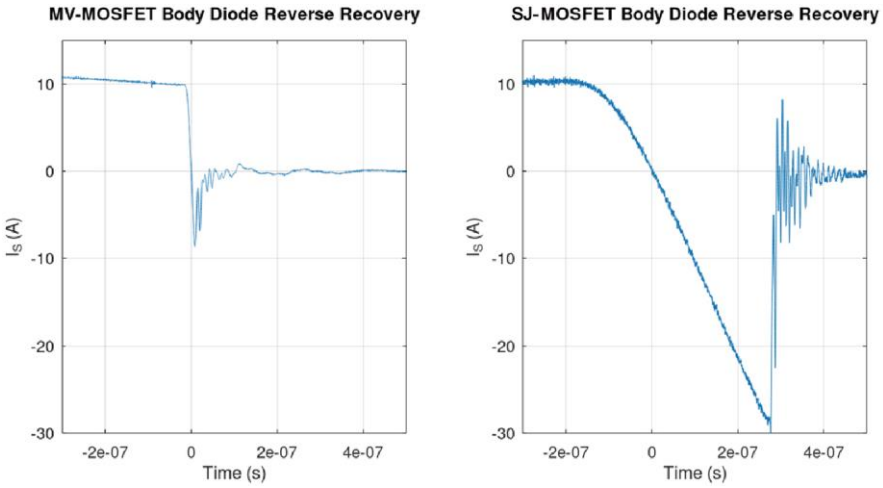

Figure 26. Body diode reverse recovery waveform of MV- and SJ-MOSFETs

Such characteristic is the reason why circuit that requires constant body diode commutation (such as synchronous buck or inverter) are completely avoided for SJ-MOSFET application. And only use the SJ-MOSFET for application where body diode commutation is not possible by design (e.g. boost PFC) or where body diode commutation occurs only for short duration and at a certain condition (for example on a ZVS converter such as LLC or phase shift full bridge during light load, soft-start, or large load transient). Careful design is required to ensure dI/dt during body diode commutation and the duration of hard commutation is short as possible.

6 Conclusions

The MOSFET datasheet parameters has been explained in detail. The definition of the parameters, the measurement circuit, and its use for circuit design has been presented.

Nevertheless, different manufacturer has their own different definition, measurement circuit, calculation method, limit/criteria for their datasheet. Thus this application note should only be used as a general information to help understand the device characteristic.

7 References

[1] PANJIT International Inc., “PJMF390N65EC - Datasheet,” October 2021.

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