

**100V N-Channel Enhancement Mode MOSFET**

<b>Voltage</b>	<b>100 V</b>	<b>R<sub>DS(ON)</sub></b>	<b>2.8 mΩ</b>
<b>Current</b>	<b>240 A</b>	<b>Q<sub>G</sub> (TYP)</b>	<b>65 nC</b>

**Feature**

- R<sub>DS(ON)</sub> < 2.8 mΩ at V<sub>GS</sub> = 10 V, I<sub>D</sub> = 70 A
- R<sub>DS(ON)</sub> < 4.2 mΩ at V<sub>GS</sub> = 6 V, I<sub>D</sub> = 35 A
- High switching speed
- Low reverse transfer capacitance
- Lead free in compliance with EU RoHS 2.0
- Green molding compound as per IEC 61249 standard
- 100% UIS / Rg test in mass production

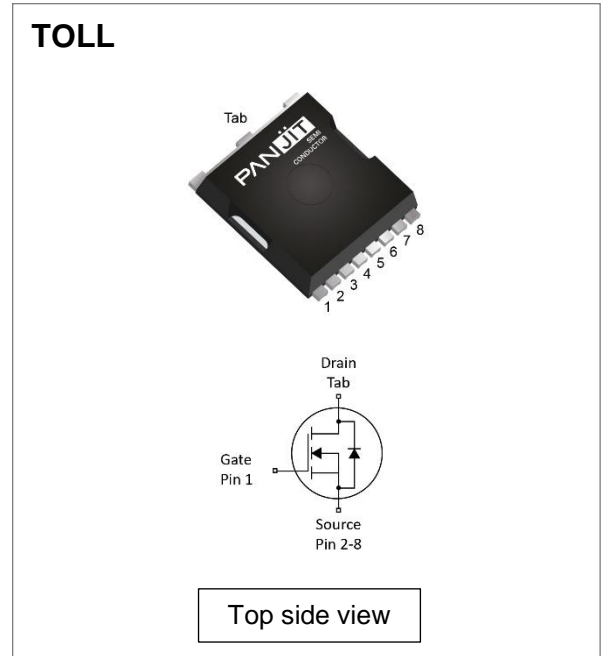
**Mechanical Data**

- Case: TOLL Package
- Approx. Weight: 0.775 grams

**Application**

- ESS / BBU/ LEV / BSG.

**Absolute Maximum Ratings** (T<sub>A</sub> = 25 °C unless otherwise specified)



PARAMETER		SYMBOL	LIMIT	UNITS
Drain-Source Voltage		V <sub>DS</sub>	100	V
Gate-Source Voltage		V <sub>GS</sub>	±20	
Continuous Drain Current by R <sub>θJC</sub> (Note 3)	T <sub>C</sub> =25 °C	I <sub>D</sub>	240	A
	T <sub>C</sub> =100 °C		168	
Continuous Drain Current by R <sub>θJA</sub>	T <sub>A</sub> =25 °C	I <sub>D</sub>	25.5	A
	T <sub>A</sub> =70 °C		21	
Pulsed Drain Current by R <sub>θJC</sub>		I <sub>DM</sub>	960	A
Single Pulse Avalanche Current (Note 5)		I <sub>AS</sub>	70	A
Single Pulse Avalanche Energy (Note 5)		E <sub>AS</sub>	245	mJ
Power Dissipation by R <sub>θJC</sub>	T <sub>C</sub> =25 °C	P <sub>D</sub>	333	W
	T <sub>C</sub> =100 °C		167	
Power Dissipation by R <sub>θJA</sub>	T <sub>A</sub> =25 °C	P <sub>D</sub>	3.8	W
	T <sub>A</sub> =70 °C		2.6	
Operating Junction and Storage Temperature Range		T <sub>J</sub> , T <sub>STG</sub>	-55~175	°C

**Thermal Characteristics**

PARAMETER	SYMBOL	VALUES			UNITS	
		MIN.	TYP.	MAX.		
Thermal Resistance	Junction-to-Case (Bottom)	R <sub>θJC</sub>	-	0.3	0.45	°C/W
	Junction-to-Ambient (Note 4)	R <sub>θJA</sub>	-	-	40	°C/W

## Electrical Characteristics (T<sub>A</sub> = 25 °C unless otherwise specified)

PARAMETER	SYMBOL	TEST CONDITION	MIN.	TYP.	MAX.	UNITS
<b>Static Characteristics</b>						
Drain-Source Breakdown Voltage	BV <sub>DSS</sub>	V <sub>GS</sub> =0 V, I <sub>D</sub> =250 μA	100	-	-	V
Gate Threshold Voltage	V <sub>GS(th)</sub>	V <sub>DS</sub> =V <sub>GS</sub> , I <sub>D</sub> =440 μA	1.8	2.8	3.8	
Drain-Source On-State Resistance (Note 1)	R <sub>DS(on)</sub>	V <sub>GS</sub> =10 V, I <sub>D</sub> =70 A	-	2.4	2.8	mΩ
		V <sub>GS</sub> =6 V, I <sub>D</sub> =35 A	-	3.2	4.2	
Zero Gate Voltage Drain Current	I <sub>DSS</sub>	V <sub>DS</sub> =100 V, V <sub>GS</sub> =0 V	-	-	2	μA
Gate-Source Leakage Current	I <sub>GSS</sub>	V <sub>GS</sub> =±20 V, V <sub>DS</sub> =0 V	-	-	±100	nA
Transfer characteristics (Note 1)	g <sub>fs</sub>	V <sub>DS</sub> =10 V, I <sub>D</sub> =70 A	-	160	-	S
<b>Dynamic Characteristics (Note 6)</b>						
Total Gate Charge	Q <sub>g</sub>	V <sub>DS</sub> =50 V, I <sub>D</sub> =70 A, V <sub>GS</sub> =10 V	-	65	85	nC
Gate-Source Charge	Q <sub>gs</sub>		-	23	-	
Gate-Drain Charge	Q <sub>gd</sub>		-	9.3	-	
Gate Plateau Voltage	V <sub>plateau</sub>		-	4.5	-	V
Input Capacitance	C <sub>iss</sub>	V <sub>DS</sub> =50 V, V <sub>GS</sub> =0 V, f=250 kHz	-	4540	5900	pF
Output Capacitance	C <sub>oss</sub>		-	1980	2570	
Reverse Transfer Capacitance	C <sub>rss</sub>		-	14	-	
Output Charge	Q <sub>oss</sub>	V <sub>DS</sub> =50 V, V <sub>GS</sub> =0 V	-	145	190	nC
Turn-On Delay Time	t <sub>d(on)</sub>	V <sub>DD</sub> =50 V, I <sub>D</sub> =70 A, V <sub>GS</sub> =10 V, R <sub>G</sub> =1.8 Ω (Note 2)	-	17.1	-	ns
Rise Time	t <sub>r</sub>		-	6.0	-	
Turn-Off Delay Time	t <sub>d(off)</sub>		-	27.4	-	
Fall Time	t <sub>f</sub>		-	5.4	-	
Gate Resistance	R <sub>g</sub>	f =1.0 MHz	-	0.5	1.0	Ω
<b>Drain-Source Diode</b>						
Diode Forward Voltage	V <sub>SD</sub>	I <sub>S</sub> =70 A, V <sub>GS</sub> =0 V	-	0.9	1.2	V
Reverse Recovery Charge	Q <sub>rr</sub>	I <sub>F</sub> =70 A, V <sub>DD</sub> =50 V, di/dt=100 A/μs	-	86	-	nC
Reverse Recovery Time	T <sub>rr</sub>		-	184	-	ns

### NOTES :

1. Pulse width ≤ 300 μs, Duty cycle ≤ 2 %.
2. Essentially independent of operating temperature typical characteristics.
3. The maximum drain current calculated by maximum junction temperature and thermal impedance. It can be varied by application and environment.
4. R<sub>θJA</sub> is the sum of the junction-to-case and case-to-ambient thermal resistance where the case thermal reference is defined as the solder mounting surface of the drain pins. Mounted on a 1 inch<sup>2</sup> with 2oz.square pad of copper.
5. E<sub>AS</sub> is calculated based on the condition of L = 0.1 mH, I<sub>AS</sub> = 70 A, V<sub>DD</sub> = 50 V, V<sub>GS</sub> = 10 V and 100% test in production.
6. Guaranteed by design, not subject to production testing.

TYPICAL CHARACTERISTIC CURVES

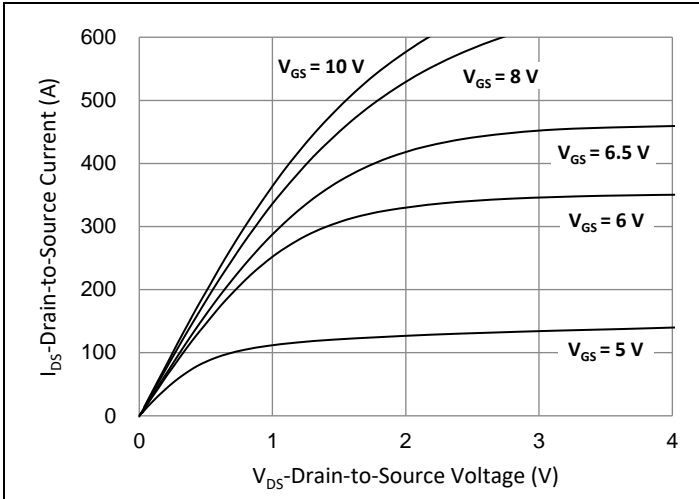


Fig.1 Output Characteristics

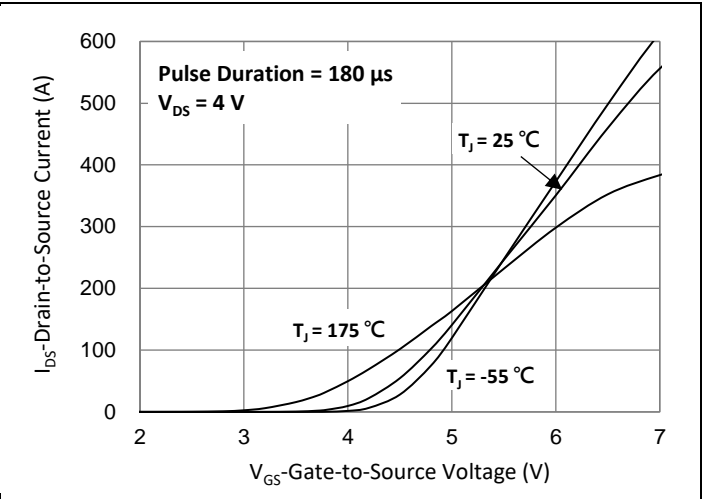


Fig.2 Transfer Characteristics

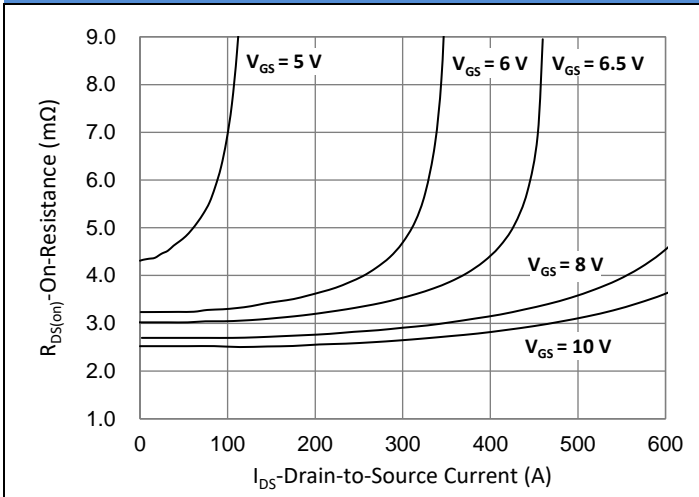


Fig.3 On-Resistance vs. Drain Current

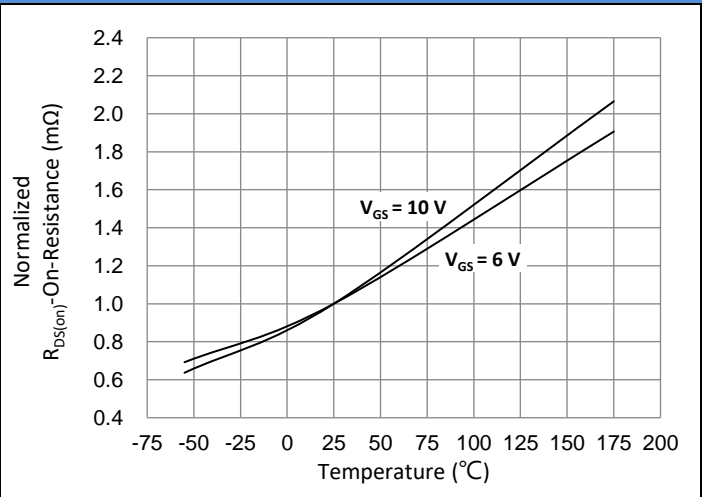


Fig.4 On-Resistance vs. Junction temperature

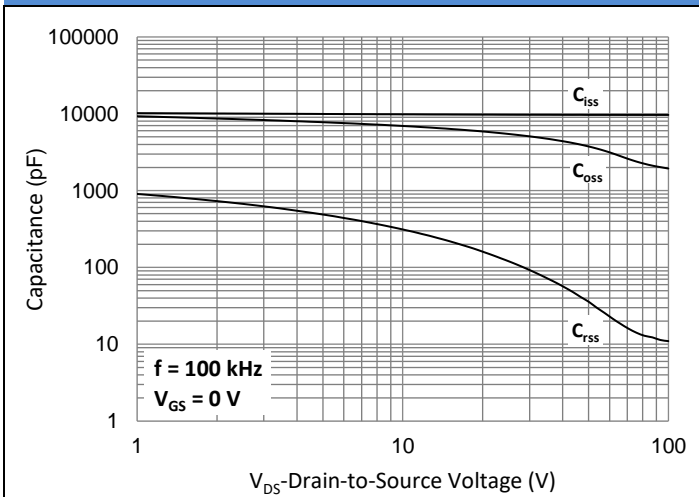


Fig.5 Capacitance vs. Drain-Source Voltage

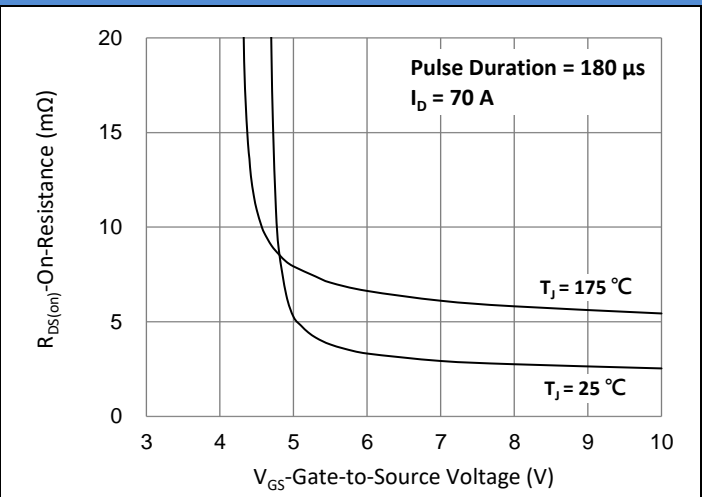


Fig.6 On-Resistance vs. Gate-Source Voltage

TYPICAL CHARACTERISTIC CURVES

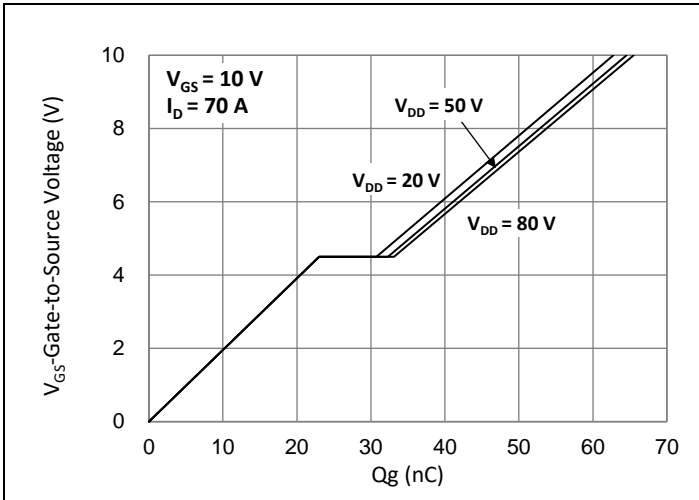


Fig.7 Gate-Charge Characteristics

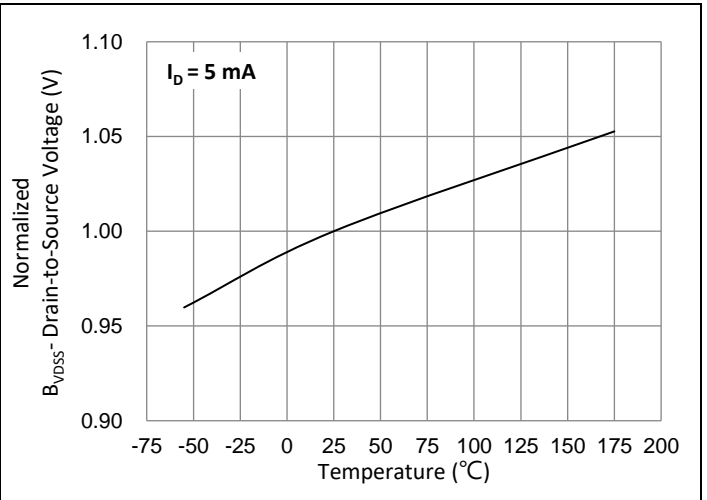


Fig.8 Breakdown Voltage Variation vs. Temperature

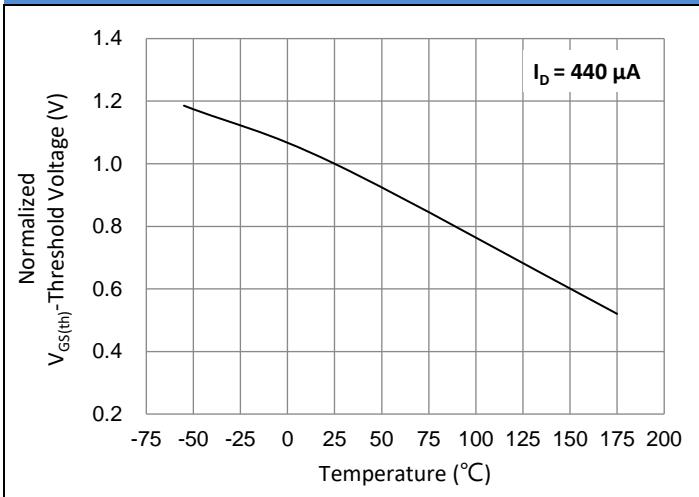


Fig.9 Threshold Voltage Variation with Temperature

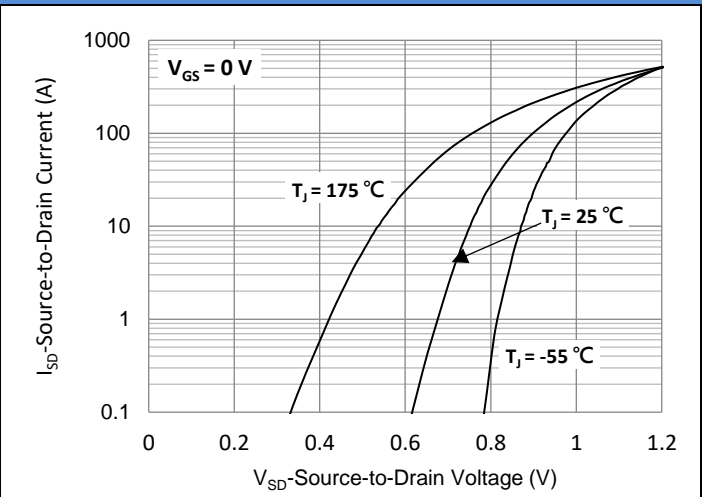


Fig.10 Source-Drain Diode Forward Voltage

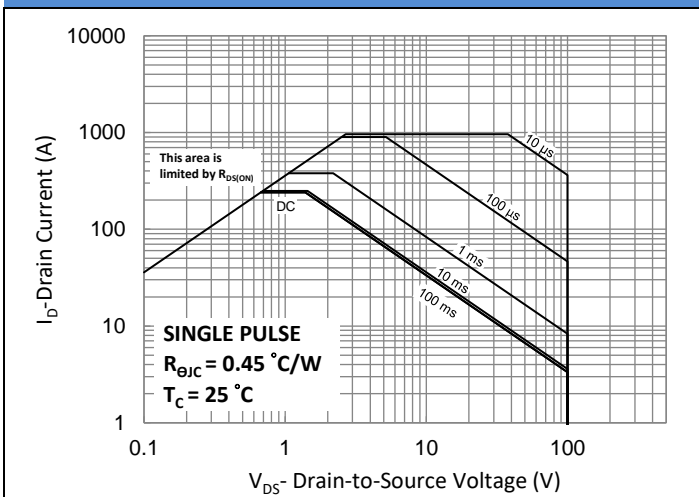


Fig.11 Maximum Safe Operating Area

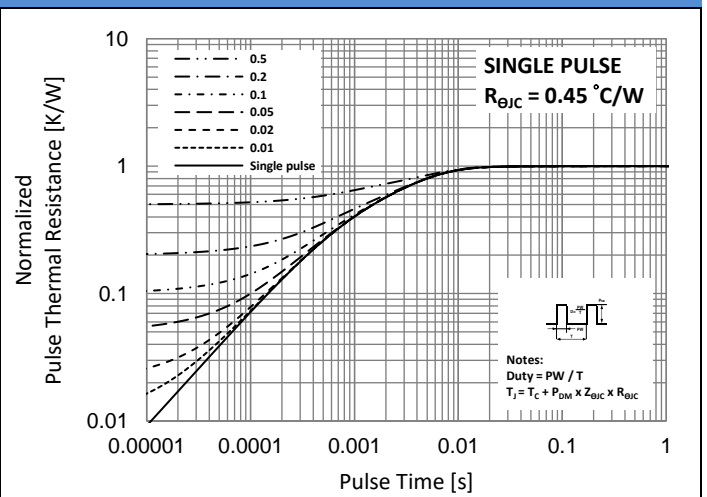
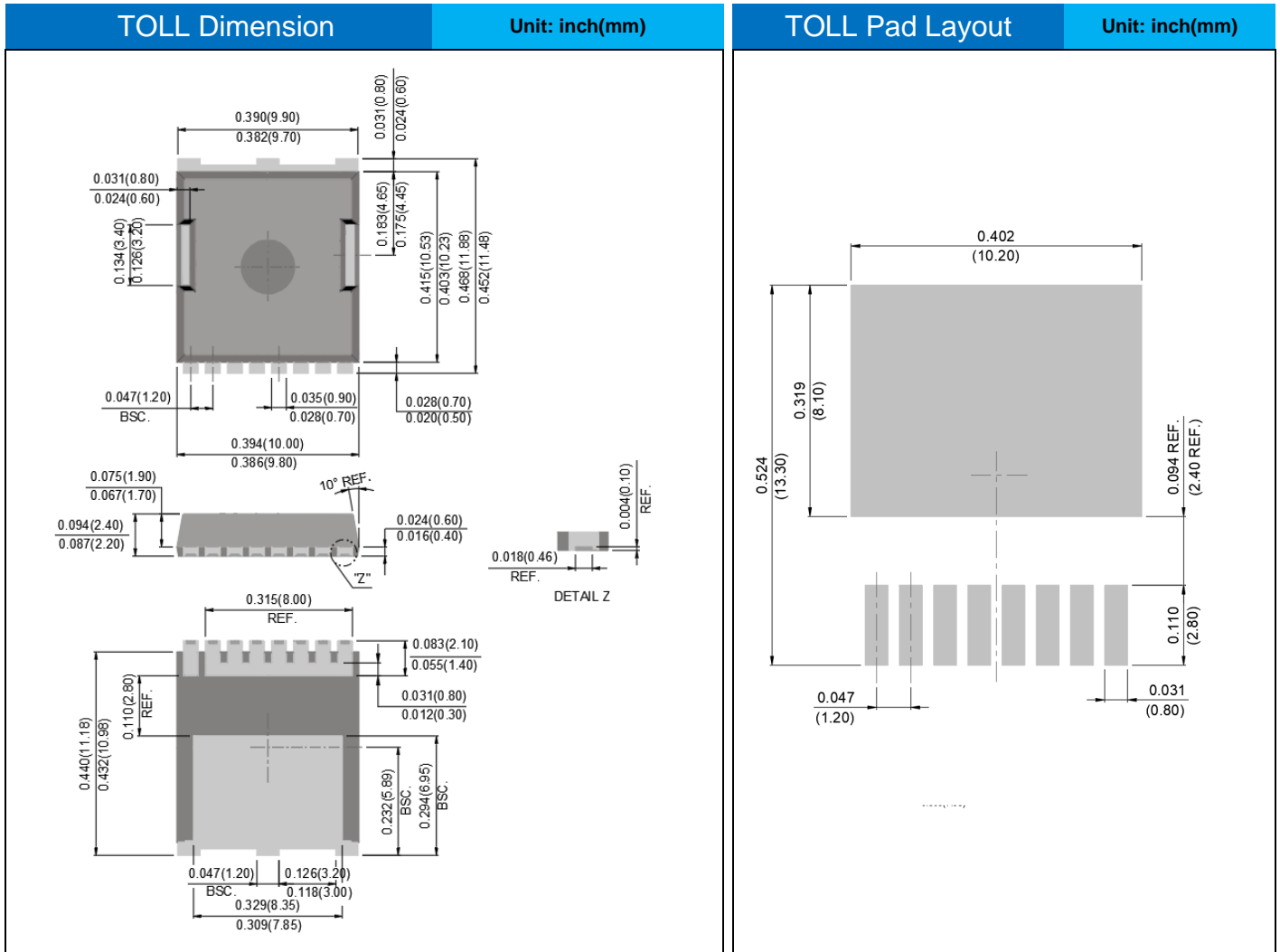


Fig.12 Normalized Transient Thermal Impedance

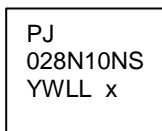
**Product and Packing Information**

Part No.	Package Type	Packing Type	Marking
PSMN028N10NS2	TOLL	2000pcs / 13"reel	028N10NS

**Packaging Information & Mounting Pad Layout**



**Marking Diagram**



- Y** = Year Code
- W** = Week Code (A~Z)
- LL** = Lot Code (00~99)
- x** = Production Line Code

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