

60V N-Channel Enhancement Mode MOSFET

Voltage **60 V** **R_{DS(ON)}** **3.3 mΩ**

Current **131 A** **Q_G (TYP)** **99 nC**

Feature

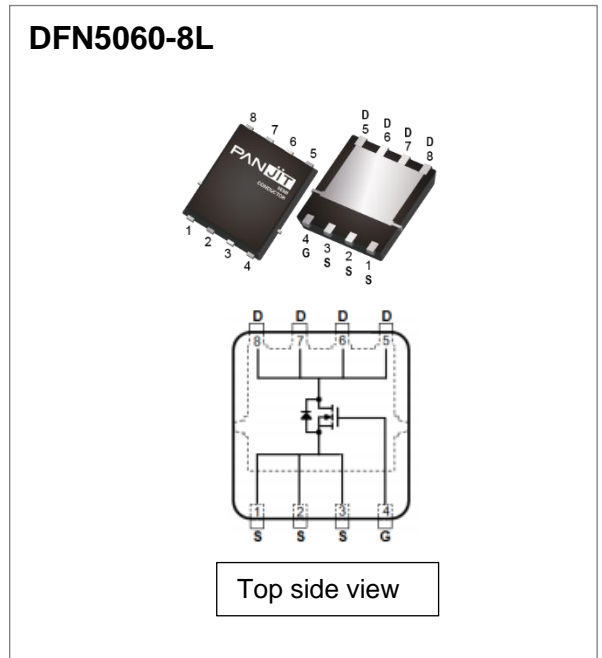
- R_{DS(ON)}, V_{GS}@10V, I_D@40A<3.3mΩ
- R_{DS(ON)}, V_{GS}@7V, I_D@10A<5.4mΩ
- High switching speed
- Low reverse transfer capacitance
- Lead free in compliance with EU RoHS 2.0
- Green molding compound as per IEC 61249 standard

Mechanical Data

- Case: DFN5060-8L Package
- Terminals: Solderable per MIL-STD-750, Method 2026
- Approx. Weight: 0.0028 ounces, 0.08 grams

Application

- BMS, BLDC motor driver switch, Load Switch.



Absolute Maximum Ratings (T_A = 25 °C unless otherwise specified)

PARAMETER	SYMBOL	LIMIT	UNITS
Drain-Source Voltage	V _{DS}	60	V
Gate-Source Voltage	V _{GS}	+20/ -12	
Continuous Drain Current (Note 3)	I _D	T _C =25°C	131
		T _C =100°C	83
Pulsed Drain Current	I _{DM}	524	A
Single Pulse Avalanche Current (Note 5)	I _{AS}	62	A
Single Pulse Avalanche Energy (Note 5)	E _{AS}	192	mJ
Power Dissipation	P _D	T _C =25°C	96
		T _C =100°C	38
Operating Junction and Storage Temperature Range	T _J , T _{STG}	-55~150	°C

Thermal Characteristics

PARAMETER	SYMBOL	MAXIMUM	UNITS
Thermal Resistance	Junction-to-Case (Bottom)	R _{θJC}	1.3
	Junction-to-Case (Top)	R _{θJT}	21
	Junction-to-Ambient (Note.4)	R _{θJA}	50

Electrical Characteristics ($T_A = 25^\circ\text{C}$ unless otherwise specified)

PARAMETER	SYMBOL	TEST CONDITION	MIN.	TYP.	MAX.	UNITS
Static						
Drain-Source Breakdown Voltage	BV_{DSS}	$V_{GS}=0V, I_D=250\mu A$	60	-	-	V
Gate Threshold Voltage	$V_{GS(th)}$	$V_{DS}=V_{GS}, I_D=250\mu A$	2	3	4	
Drain-Source On-State Resistance (Note 1)	$R_{DS(on)}$	$V_{GS}=10V, I_D=40A$	-	2.5	3.3	m Ω
		$V_{GS}=7V, I_D=10A$	-	3.2	5.4	
Zero Gate Voltage Drain Current	I_{DSS}	$V_{DS}=60V, V_{GS}=0V$	-	-	1	μA
Gate-Source Leakage Current	I_{GSS}	$V_{GS}=20V, V_{DS}=0V$	-	-	100	nA
Transfer characteristics (Note 1)	gfs	$V_{DS}=3V, I_D=20A$	-	71	-	S
Dynamic (Note 6)						
Total Gate Charge	Q_g	$V_{DS}=30V, I_D=40A,$ $V_{GS}=7V$	-	74	-	nC
			-	99	-	
Gate-Source Charge	Q_{gs}	$V_{DS}=30V, I_D=40A,$ $V_{GS}=10V$	-	26	-	
Gate-Drain Charge	Q_{gd}		-	29	-	
Plateau Voltage	V_{GP}		-	4.8	-	V
Input Capacitance	C_{iss}	$V_{DS}=30V, V_{GS}=0V,$ $f=1.0\text{MHz}$	-	5731	-	pF
Output Capacitance	C_{oss}		-	2070	-	
Reverse Transfer Capacitance	C_{rss}		-	120	-	
Turn-On Delay Time	$t_{d(on)}$	$V_{DD}=30V, I_D=40A,$ $V_{GS}=10V, R_G=2\Omega$ (Note 2)	-	61	-	ns
Turn-On Rise Time	t_r		-	106	-	
Turn-Off Delay Time	$t_{d(off)}$		-	106	-	
Turn-Off Fall Time	t_f		-	59	-	
Gate Resistance	R_g	$f = 1.0\text{MHz}$	0.5	1.7	3	Ω
Drain-Source Diode						
Diode Forward Voltage	V_{SD}	$I_S=1A, V_{GS}=0V$	-	0.7	1	V
Reverse Recovery Charge	Q_{rr}	$I_{SD} = 40A$ $di/dt = 100A/\mu s$	-	42	-	nC
Reverse Recovery Time	T_{rr}		-	52	-	ns

NOTES :

1. Pulse width $\leq 300\mu s$, Duty cycle $\leq 2\%$
2. Essentially independent of operating temperature typical characteristics.
3. The maximum current rating is silicon limited.
4. $R_{\theta JA}$ is the sum of the junction-to-case and case-to-ambient thermal resistance where the case thermal reference is defined as the solder mounting surface of the drain pins. Mounted on a 1 inch² with 2oz.square pad of copper.
5. The test condition is $L=0.1\text{mH}$, $I_{AS}=62A$, $V_{DD}=25V$, $V_{GS}=10V$, $R_G=25\text{ohm}$, Starting $T_J=25^\circ\text{C}$
6. Guaranteed by design, not subject to production testing.

TYPICAL CHARACTERISTIC CURVES

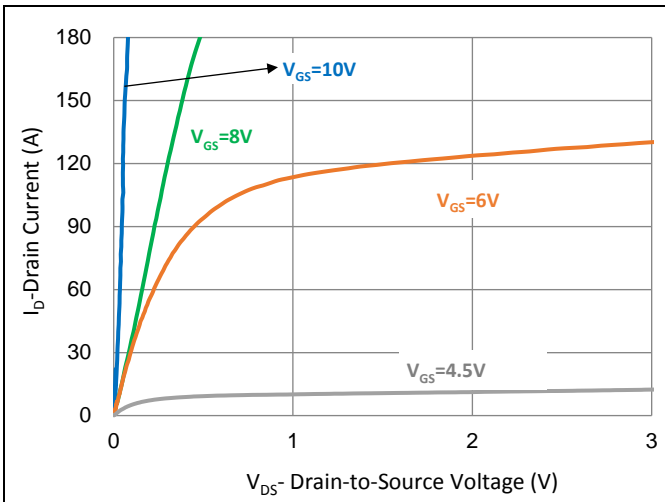


Fig.1 Output Characteristics

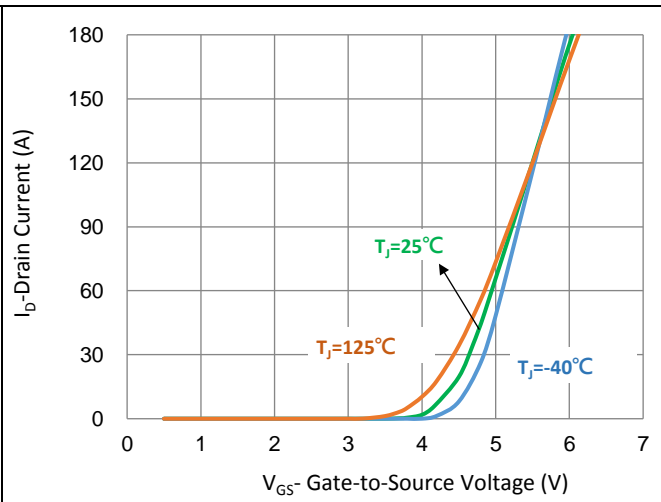


Fig.2 Transfer Characteristics

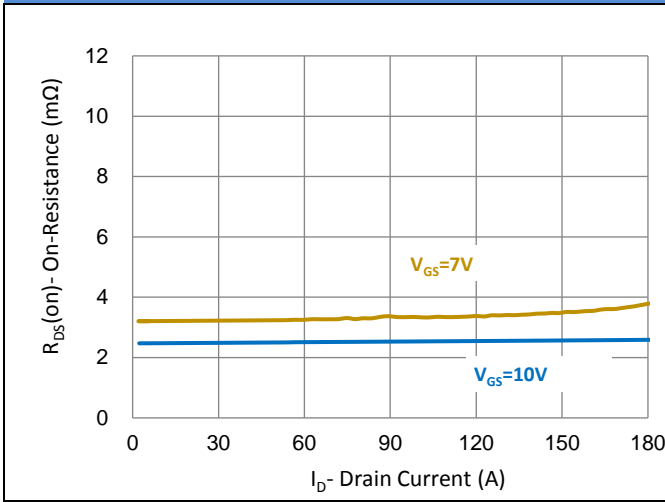


Fig.3 On-Resistance vs. Drain Current

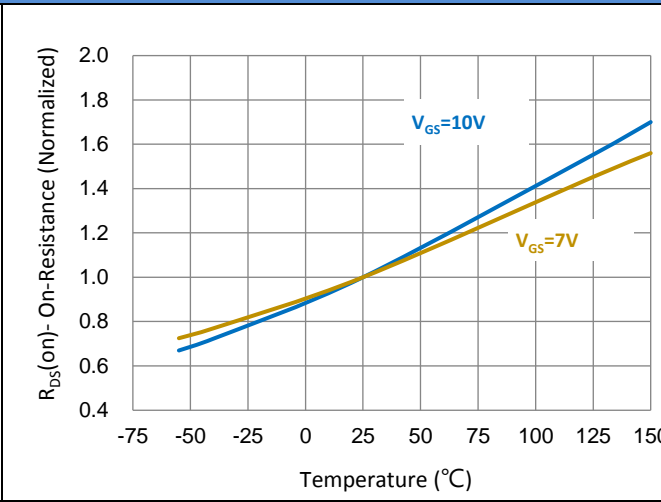


Fig.4 On-Resistance vs. Junction temperature

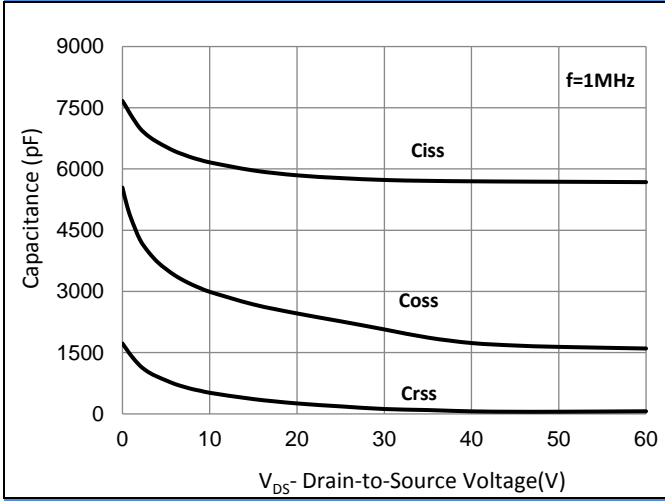


Fig.5 Capacitance vs. Drain-Source Voltage

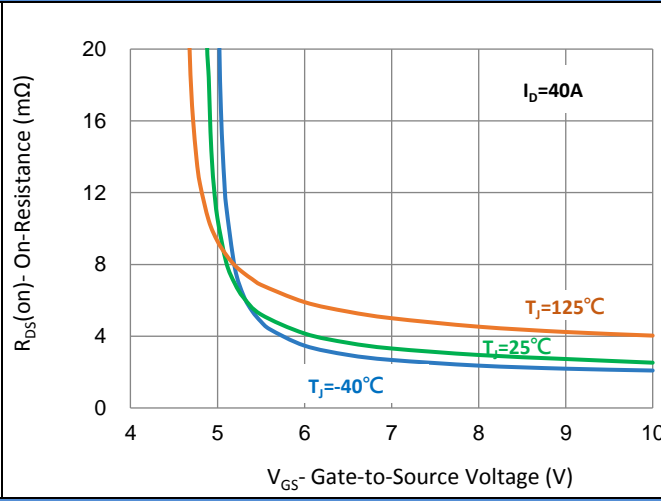


Fig.6 On-Resistance vs. Gate-Source Voltage

TYPICAL CHARACTERISTIC CURVES

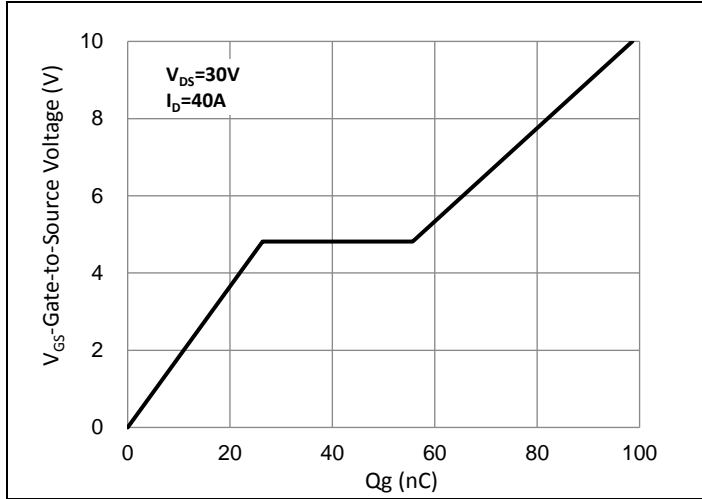


Fig.7 Gate-Charge Characteristics

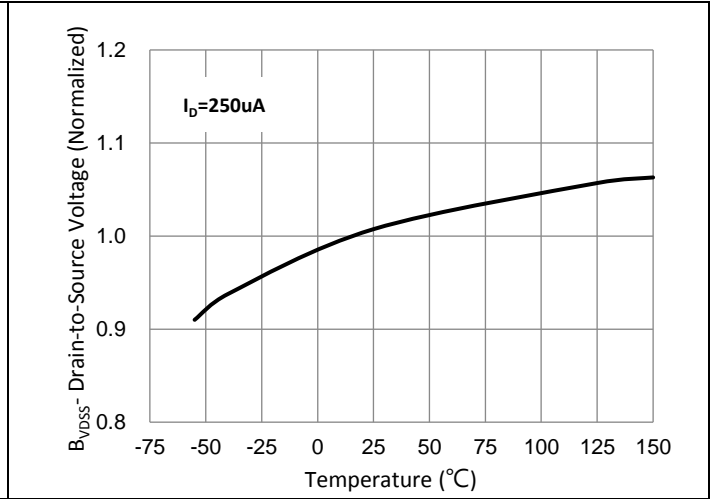


Fig.8 Breakdown Voltage Variation vs. Temperature

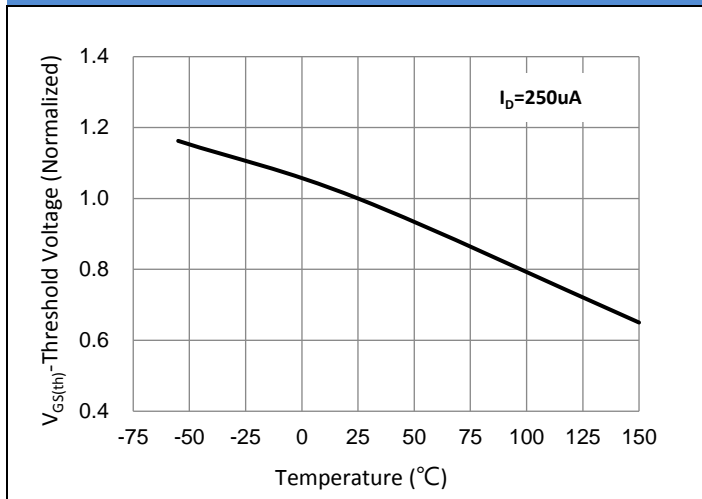


Fig.9 Threshold Voltage Variation with Temperature

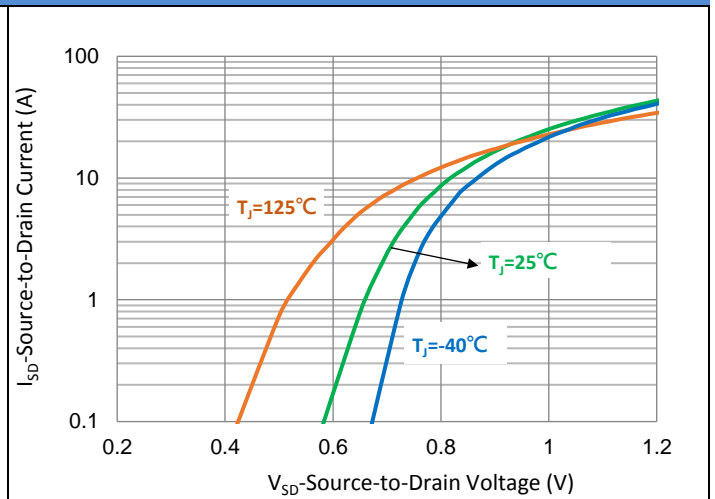


Fig.10 Source-Drain Diode Forward Voltage

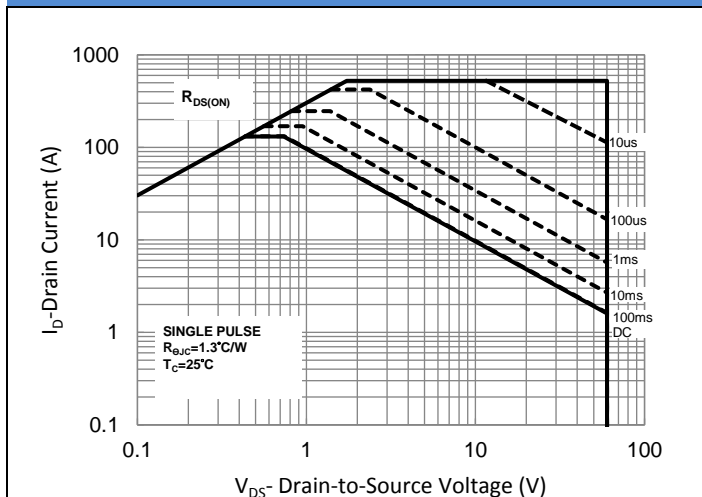


Fig.11 Maximum Safe Operating Area

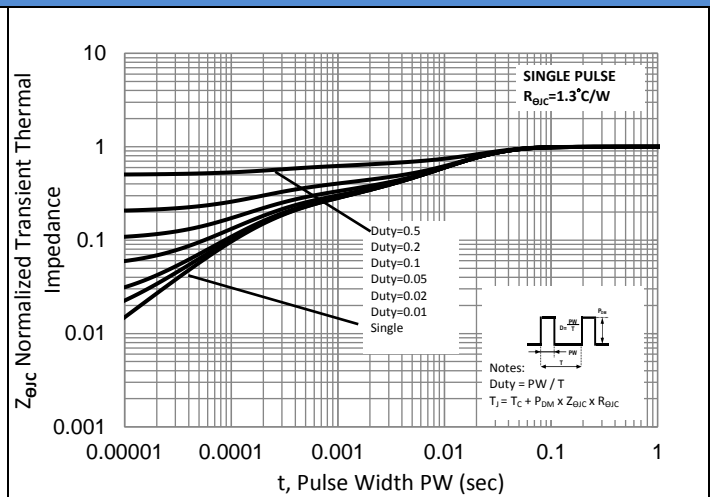


Fig.12 Normalized Transient Thermal Impedance

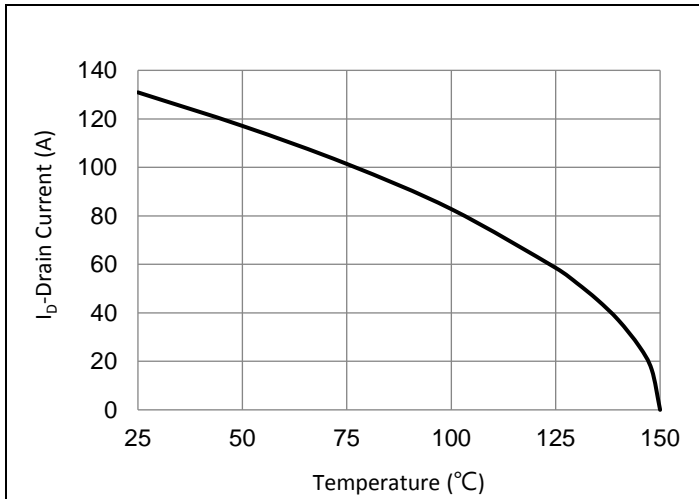
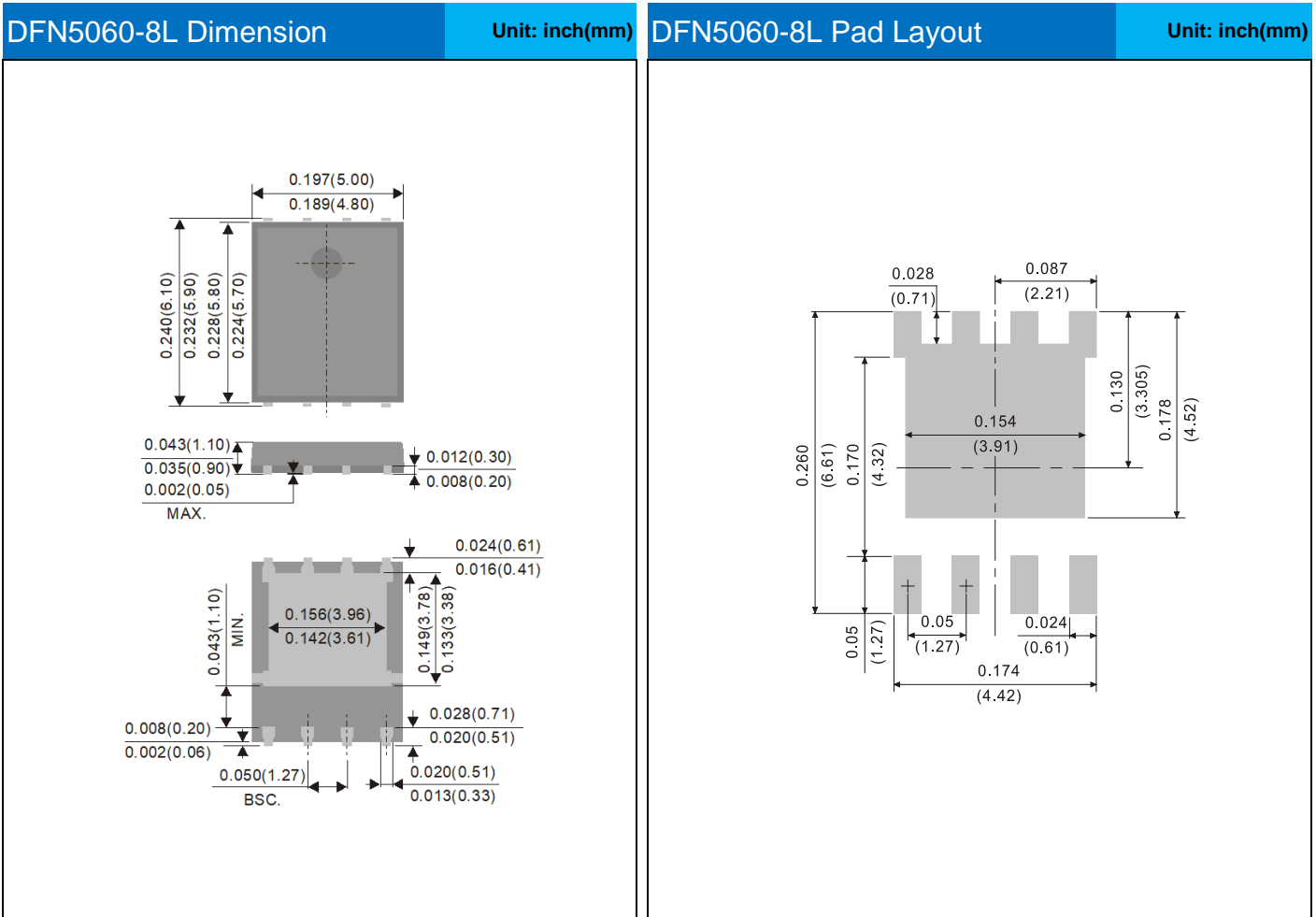


Fig.13 Drain Current vs. Case Temperature

Product and Packing Information

Part No.	Package Type	Packing Type	Marking
PSMQC033N06NS1	DFN5060-8L	3000pcs / 13" reel	033N06NS

Packaging Information & Mounting Pad Layout



Marking Diagram

PJ 033N06NS YWLL x

- Y** = Year Code
- W** = Week Code (A~Z)
- LL** = Lot Code (00~99)
- x** = Production Line Code

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