PJ39900i-M0 Datasheet

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Contents

1 Introduction

The document is the datasheet of PJ39900i-M0 series.

Users can refer to the "PJ39900i User Manual" for further understanding of the functionality of PJ39900i-M0.

2 Product Description

The PJ39900i-M0 MCU utilizes an ARM® Cortex®-M0 core, with a maximum operating frequency of 48 MHz. It features built-in 16 KBytes of Flash, 256 Bytes of EEPROM, and 4 KBytes of SRAM. By configuring the Flash controller registers, interrupt vectors can be remapped within the 16 KByte space.

With the exception of power and ground pins, all pins of the PJ39900i-M0 MCU can function as GPIO, peripheral IO, or external interrupt inputs. In applications with limited pin count, the MCU provides as many pin signals as possible.

The PJ39900i-M0 MCU is equipped with multiple communication interfaces:

- **1 route high-speed (up to 4 Mbit/s) USART**

  The USART supports synchronous and asynchronous full-duplex or half-duplex communication, multi-master communication, LIN protocol, Smart-Card protocol, IrDA SIR encoding/decoding; it allows the software interchange the pin positions of RX and TX; in MCU stop-mode (Stop), it supports to wake up by data reception.

- **1 route high-speed (up to 16 Mbit/s) SPI/I2S**

  The SPI/I2S supports full-duplex or half-duplex communication with data length ranging from 4 to 16 bits, master/slave mode, TI mode, NSS pulse mode, automatic CRC checksum, and I2S protocol.

- **1 route high-speed (up to 1 Mbit/s) I2C**

  I2C supports 1 Mbit/s, 400 Kbit/s, 100 Kbit/s transmission rate, master/slave mode, multi-master mode, 7/10 bits addressing and SMBus protocol. In MCU stop-mode (Stop), it supports to wake up by data reception.

The PJ39900i-M0 MCU features a 16-bit advanced PWM timer (with 4 outputs of PWM, including 3 outputs with dead-time with complementary), a 16-bit general-purpose PWM timer (with 4 outputs of PWM), and a 16-bit basic timer (for timing CPU interrupts).

The PJ39900i-M0 MCU integrates the following analog circuits: one 12-bit 1 MSPS ADC (effective resolution of 8 bits), one power-on/power-down reset (POR/PDR) circuit, one internal voltage for reference (sampled via on-chip ADC), and built-in an integrated 5V/50mA LDO, one route 3.3V/50mA LDO, and two low-offset route of operational amplifiers.

The PJ39900i-M0 MCU supports various power modes. In low-power mode, it can be automatically awakened by the internal low-power timer.

The PJ39900i-M0 MCU includes a three-phase brushless gate driver capable of operating at up to 36V, designed to drive P+N structure MOSFETs.

The PJ39900i-M0 MCU integrates three half-bridge P+N type MOSFETs with lower $R_{DS(ON)}$.

Due to its rich peripheral configuration, the PJ39900i-M0 MCU is suitable for varies applications.

- Motor driving and speed control
- UAV flight control, gimbal control

- Toy
- Home appliances
- Smart robots

2.1 Product Features

◆ **CPU Core**

- ARM® Cortex®-M0
- Maximum clock frequency：48 MHz
- 24-bit System Tick Timer
- Supports interrupt vector remapping (configured through the Flash controller's registers)

◆ **Operating Voltage Range:**

- Power：7 V ~ 24 V
- Operating temperature range：-40°C ~ +85°C
- CPU tracing and debugging
- SWD debugging interfaces
- ARM® CoreSight™ debugging components（ROM-Table, DWT, BPU）
- Custom DBGMCU debugging controller (low-power mode emulation control, debugging peripheral clock control, debugging and trace interface allocation)

◆ **Memory**

- 16 KByte Flash (128 pages, each page 128 bytes; 32-bit data read, 16-bit data write)
- The Flash memory features data security protection, with option for settings separate read and write protections
- 256 Byte EEPROM
- 4 KByte SRAM

◆ **Data Security**

- CRC check hardware unit

◆ **Clock**

- External inputs clock（GPIO）: supports 1 to 48 MHz
- High-speed Internal（HIS）: 48 MHz
- Low-speed Internal（LSI）: 114 kHz

◆ **Reset**

- External pin reset
- Power reset (POR/PDR)

- Software reset
- Watchdog (IWDG and WWDG) timer reset

◆ **GPIO Port**

- Supports up to 11 GPIO ports
- Each GPIO can function as an external interrupt input
- Built-in switchable pull-up and pull-down resistors
- Supports open-drain output
- High and low output drive capability are selectable

◆ **Data communication interface**

- 1 route high-speed (up to 4 Mbit/s) USART (MCU supports data reception wake-up in Stop mode)
- 1 route high-speed (up to 1 MHz) I2C (MCU supports data reception wake-up in Stop mode)
- 1 route high-speed (up to 16 Mbit/s) SPI (supports I2S protocol)

◆ **Timer and PWM generator**

- 1 x 16-bit advanced PWM timer (4 PWM outputs in total, with 3 channels supporting complementary output with dead zone)
- 1 x 16-bit general-purpose PWM timer (4 PWM outputs in total)
- 1 x 16-bit basic timer (supports CPU interrupts)
- 1 auto-wakeup timer (AWU), usable in MCU Stop mode

◆ **On-chip analog circuits**

- 1 x 5% accuracy 5V/50mA LDO
- 1 x 2% accuracy 3.3V/50mA LDO
- 1 x 12-bit 1 MSPS ADC (6 channels for both internal and external analog signal inputs, supports differential input pairs)
- 1 power-on/power-down reset circuit
- 1 x 0.8 V internal reference voltage (internally sampled by ADC)
- 2 route low-offset operational amplifiers, supporting millivolt-level signal amplification via current sensing resistors

◆ **Three-phase brushless gate driver**

- P+N MOS three-phase push-pull gate driver
- Output 10 V VGS available for low-side NMOS use
- Input voltage VIN undervoltage lockout protection (UVLO)
- Built-in shoot-through prevention feature

- Built-in 500 ns dead time
- High and low side channel matching

◆ **MOSFET**

- N-channel：
- VDS = 24 V， ID = 5 A
- $R_{DS(ON)}$ = 14.6 mΩ (typical) @ VGS = 10 V
- P-Channel：
- VDS = -24 V， ID = -5 A
- RDS(ON) = 47.9 mΩ (typical) @ VGS = -10 V

◆ **64-bit unique chip ID identifier**

- Each chip provides a unique 64-bit ID identifier

2.2 Device Overview

Table 2-1 PJ39900i-M0 Series Feature

Feature	PJ39900i-M0
Working voltage	7 V ~ 24 V
Operating temperature	-40°C ~ +85°C
CPU operating frequency	48 MHz
System Tick	1
Flash	16 KByte
EEPROM	256 Byte
SRAM	4 KByte
CRC	1
IWDG	1
WWDG	1
USART	1
I2C	1
SPI/I2S	1
Advanced timer	1
General-purpose timer	1
Basic timer	1
AWU (Auto-Wakeup Unit) timer	1
ADC (External channel count)	1(5)
OP	2
POR/PDR	1

Feature	PJ39900i-M0
Internal reference voltage	1
64-bit ID identifier	1
External interrupt	11
GPIO	11
Package	TSSOP-25P

3 Function Introduction

3.1 Block Diagram

The ARM® Cortex®-M0 processor is an embedded 32-bit RISC processor. It is a low-cost, low-power MCU platform that provides excellent computing performance and advanced interrupt system responsiveness. The PJ39900i-M0 MCU features a built-in Cortex®-M0 core, compatible with ARM tools and software. The diagram below illustrates the core diagram of the PJ39900i-M0 MCU.

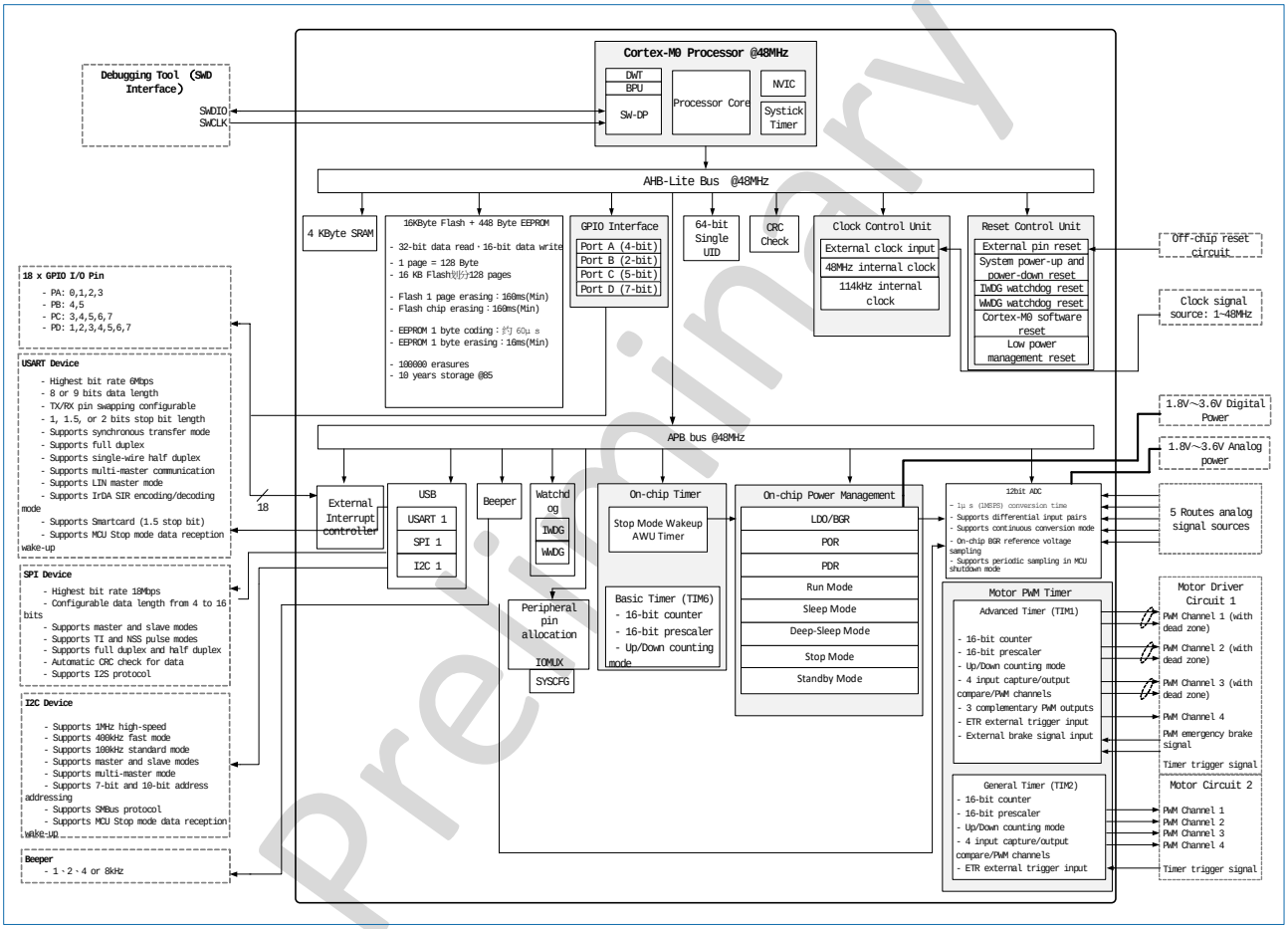

Figure 3-1 PJ39900i-M0 Block Diagram

3.2 System Block Diagram

PJ39900i-M0 is a highly integrated chip that integrates MCU, Driver, 5 V LDO, 3.3 V LDO, and three sets of P+N MOS. The internal resources and connections of PJ39900i-M0 can be observed from the system block diagram.

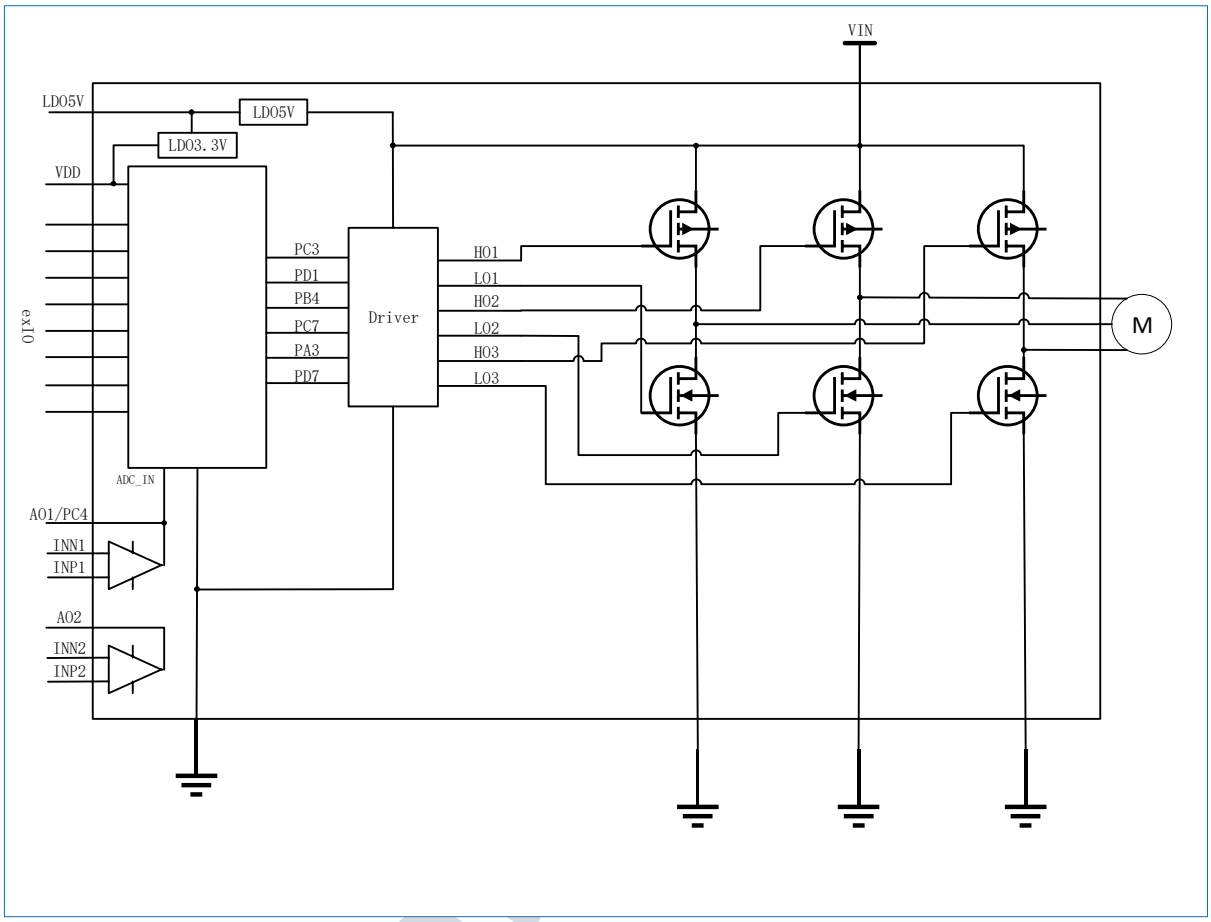

Figure 3-2 System Block Diagram

3.3 Memory Mapping Configuration

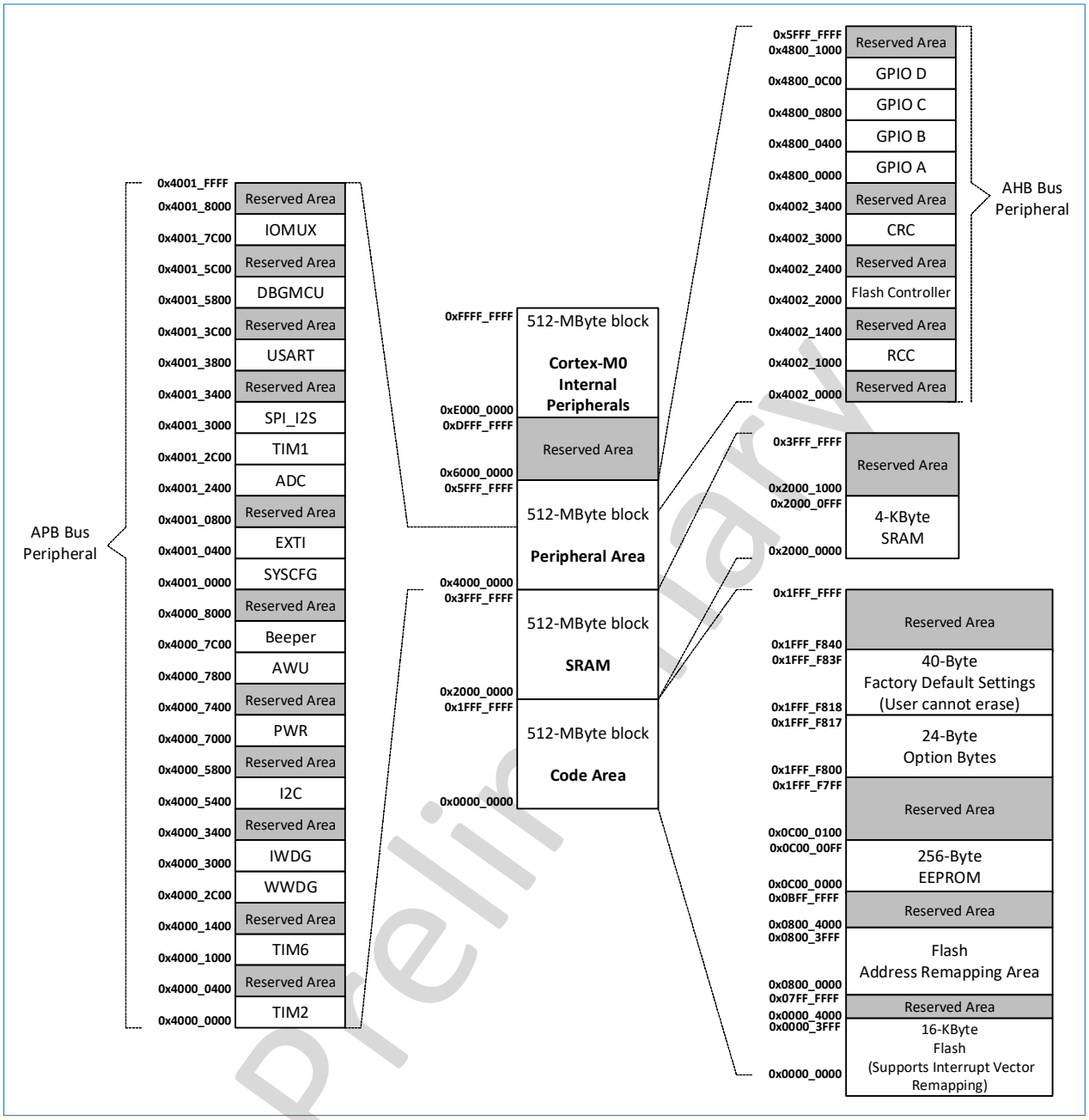

Figure 3-3 PJ39900i-M0 MCU Memory Mapping

3.3.1 Flash Features

- Flash data width: 32-bit read, 16-bit write
- Page size: 128 Byte
- Flash access width: Supports half-word (16-bit) write; 32-bit read
- Supports Flash read/write protection access control
- Interrupt vector table remapping supported through configuration registers

Table 3-1 Flash Features

	Read	Erasing and Coding
Operating Time	- LATENCY=000 and HCLK ≤ 24 MHz: 0 clock wait cycles. - LATENCY=001 and 24 MHz < HCLK ≤ 48 MHz: 1 clock wait cycle.	- Half-word write operation: approximately 60 μs - Flash page erase: approximately 160 ms (t_{erase} = 1/$f_{FLITFCLK}$*320000) - Full flash erase: approximately 160 ms (t_{erase} = 1/$f_{FLITFCLK}$*320000)
Service Time	Supports approximately 100,000 erase and read/write cycles.	

3.3.2 Flash Option Word

Table 3-2 Flash Option Word Structure

Address	[31:24]	[23:16]	[15:8]	[7:0]
0x1FFF F800	nUSER	USER	nRDP	RDP
0x1FFF F804	nDATA1	DATA1	nDATA0	DATA0
0x1FFF F808	nWRP1	WRP1	nWRP0	WRP0
0x1FFF F80C	nWRP3	WRP3	nWRP2	WRP2
0x1FFF F810	IWDG_INI_KEY[15:0]		Reserve	IWDG_RL_IV[11:0]
0x1FFF F814	DBG_CLK_CTL[15:0]		LSI_LP_CTL[15:0]	

- **IWDG_RL_IV[11:0]**：Stores the initial value of the IWDG_RLR register. When the IWDG is configured as a hardware watchdog, the IWDG_RL_IV register can be configured to set the reset interval of the IWDG.
- **IWDG_INI_KEY[15:0]**：Determines whether IWDG_RL_IV is effective. When the IWDG_INI_KEY register equals 0x5B1E, the configuration of IWDG_RL_IV takes effect; otherwise, it is invalid.
- **LSI_LP_CTL[15:0]**：Determines whether the system needs to be awakened by the IWDG cycle after enabling the IWDG and entering Stop mode.
  - If the value of LSI_LP_CTL is configured as 0x369C, the LSI can be turned off based on the LSION setting after the MCU enters Stop mode. Upon awakening, the LSI restores to its state before entering the mode.
  - If LSI_LP_CTL is not configured, the system will be awakened by the IWDG cycle after enabling the IWDG and entering Stop mode.
- **DBG_CLK_CTL[15:0]**：When the stored value is 0x12DE, it disables the CPU's internal

DEBUG clock; otherwise, it keeps the DEBUG clock enabled.

Explanation:

For the bit field definitions at addresses 0x1FFF_F800 to 0x1FFF_F80C in table 4-3, please refer to the "Flash Option Byte Register" chapter in the "MYg0002 User Manual".

3.3.3 SRAM

PJ39900i-M0 MCU integrates 4 KByte SRAM internally, supporting word, half-word, and byte read/write access. The CPU can perform fast read/write access to SRAM with zero wait cycles, meeting the requirements of most applications.

3.3.4 EEPROM

The PJ39900i-M0 MCU integrates 256 Byte EEPROM internally.

Table 3-3 EEPROM Features

	Read	Erasing and Coding
Operating Time	LATENCY=000 and HCLK ≤ 24 MHz: 0 clock wait cycles. LATENCY=001 and 24 MHz < HCLK ≤ 48 MHz: 1 clock wait cycle.	Byte programming: approximately 60 μs（t_{erase_byte}= 1/$f_{FLITFCLK}$*120） Byte erasing: approximately 16 ms（t_{erase_byte}= 1/$f_{FLITFCLK}$*32000）
Service Time	Supports approximately 100,000 erase and read/write cycles, or a lifespan of 10 years (whichever is reached first).	

3.4 CRC Calculation Unit

The Cyclic Redundancy Check (CRC) is used to verify the integrity of data transmission or storage. The PJ39900i-M0 integrates an independent CRC hardware calculation unit internally, relieving the burden on applications for user and providing accelerated processing capabilities.

During runtime, the CRC calculation unit computes the software's signature and compares it with the reference signature generated and stored at the specified storage address during linking.

3.5 NVIC

The PJ39900i-M0 features a built-in Nested Vectored Interrupt Controller (NVIC), which provides flexible interrupt management with minimal interrupt latency. The PJ39900i-M0 has a total of 11 external interrupts.

- The tightly coupled NVIC achieves low-latency interrupt response handling.
- Interrupt vector entry addresses directly enter the kernel.
- Provides a tightly coupled NVIC interface.
- Allows early handling of interrupts.
- Handles late-arriving interrupts with higher priority.

- Supports interrupt tail-chaining.
- Automatically saves processor state.
- Automatically restores upon interrupt return, without additional instruction overhead.

Table 3-4 NVIC

POSITION	priority		Name	Description	Address
-	-	-	-	reserved	0x0000 0000
-	-3	Fixed	Reset	Reset	0x0000 0004
-	-2	Fixed	NMI	Non-maskable interrupt	0x0000 0008
-	-1	Fixed	HardFault	All types of errors	0x0000 000C
-	3	Configurable	SVCall	System service dispatch via SWI instruction	0x0000 002C
-	5	Configurable	PendSV	Pendable system service request	0x0000 0038
-	6	Configurable	SysTick	System tick timer	0x0000 003C
0	7	Configurable	WWDG	Window watchdog interrupt	0x0000 0040
1	8	Configurable	-	-	0x0000 0044
2	9	Configurable	EXTI11	Automatic wake-up interrupt of EXTI line 11 (AWU_WKP)	0x0000 0048
3	10	Configurable	Flash	Flash global interrupt	0x0000 004C
4	11	Configurable	RCC	RCC global interrupt	0x0000 0050
5	12	Configurable	EXTI0	EXTI line 0 interrupt	0x0000 0054
6	13	Configurable	EXTI1	EXTI line 1 interrupt	0x0000 0058
7	14	Configurable	EXTI2	EXTI line 2 interrupt	0x0000 005C
8	15	Configurable	EXTI3	EXTI line 3 interrupt	0x0000 0060
9	16	Configurable	EXTI4	EXTI line 4 interrupt	0x0000 0064
10	17	Configurable	EXTI5	EXTI line 5 interrupt	0x0000 0068
11	18	Configurable	TIM1_BRK	TIM1 brake interrupt	0x0000 006C
12	19	Configurable	ADC	ADC interrupt (shared with EXTI line 8)	0x0000 0070
13	20	Configurable	TIM1_UP_TRG_COM	TIM1 update, trigger, and communication interrupts	0x0000 0074
14	21	Configurable	TIM1_CC	TIM1 capture/compare interrupt	0x0000 0078
15	22	Configurable	TIM2	TIM2 global interrupt	0x0000 007C
16	23	Configurable	-	-	0x0000 0080
17	24	Configurable	TIM6	TIM6 global interrupt	0x0000 0084
18	25	Configurable	-	-	0x0000 0088
19	26	Configurable	-	-	0x0000 008C
20	27	Configurable	-	-	0x0000 0090
21	28	Configurable	EXTI6	EXTI line 6 interrupt	0x0000 0094
22	29	Configurable	EXTI7	EXTI line 7 interrupt	0x0000 0098
23	30	Configurable	I2C	I2C global interrupt (shared with EXTI line 10)	0x0000 009C
24	31	Configurable	-	-	0x0000 00A0

POSITION	priority		Name	Description	Address
25	32	Configurable	SPI	SPI global interrupt	0x0000 00A4
26	33	Configurable	-	-	0x0000 00A8
27	34	Configurable	USART	USART global interrupt (shared with EXTI line 9)	0x0000 00AC
28	35	Configurable	-	-	0x0000 00B0
29	36	Configurable	-	-	0x0000 00B4
30	37	Configurable	-	-	0x0000 00B8
31	38	Configurable	-	-	0x0000 00BC

3.6 EXTI

The PJ39900i-M0 MCU features 11 built-in external interrupt (EXTI) ports. Among them, EXTI 0 to EXTI 7 are connected to IOs, while the remaining EXTI ports are connected to the following events:

- EXTI 8 is connected to the ADC's AWD event
- EXTI 9 is connected to USART's wakeup event
- EXTI 10 is connected to I2C's wakeup event
- EXTI 11 is connected to AWU's wakeup event

EXTI 8 to 10 serve as internal events, without RTSR, FTSR, SWIER, and PR registers. They can only capture the rising edge of events in Stop mode to generate ERQ and IRQ signals to wake up the system.

3.7 Reset

The PJ39900i-M0 MCU supports two reset modes: system reset and power reset.

3.7.1 System Reset

In addition to the reset flags in the clock controller's RCC_CSR register and registers in the backup area, the system reset resets all registers to their reset state. A system reset occurs when any of the following events happen:

- Low level on the NRST pin (external reset)
- Window watchdog counter termination (WWDG reset)
- Independent watchdog counter termination (IWDG reset)
- Software reset (SW reset): Achieved by setting the SYSRESETREQ bit to '1' in the Cortex®-M0 interrupt and reset control register.
- Low-power management reset

Users can identify the source of the reset event by checking the reset status flags in the RCC_CSR control status register.

For more details, please refer to the diagram below:

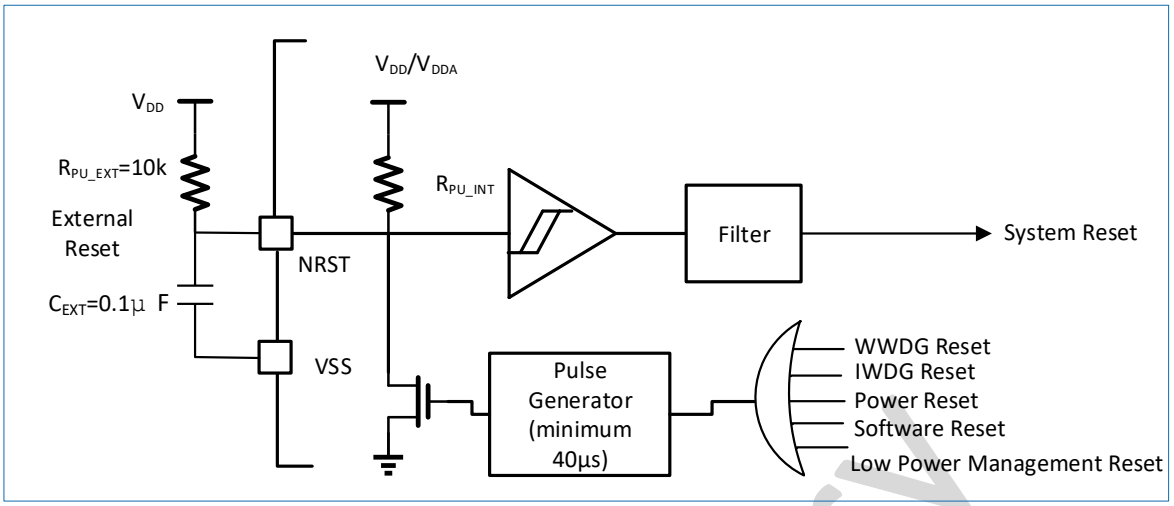

Figure 3-4 Reset Circuit

The reset source ultimately affects the NRST pin, maintaining a low level during the reset process. The reset vector entry is fixed at address 0x0000 0004.

Internal reset signals within the chip are output on the NRST pin. A pulse generator ensures that each internal reset source has a pulse delay of at least 40 μs. When the NRST pin is pulled low to generate an external reset, it will produce a reset pulse.

3.7.2 Power Reset

A power reset occurs during the following events:

- Power on/off reset (POR/PDR)

A power reset resets all registers except those in the backup area.

The PJ39900i-M0 MCU integrates a power-on reset (POR) / power-down reset (PDR) circuit internally. This circuit is always operational to ensure the system operates normally when powered above the POR/PDR threshold. When VDD is below the POR/PDR threshold, the MCU will be reset without the need for an external reset circuit.

3.8 Clock

During startup, the PJ39900i-M0 MCU selects the system clock. Upon reset, the internal 32 MHz HSI RC is the default CPU clock, and subsequently, the LSI clock can be selected as the CPU clock.

The PJ39900i-M0 MCU also provides LSI, GPIO input as clock sources, making it suitable for low-power, cost-effective design schemes.

3.8.1 Clock Source

Table 3-5 Clock Source

HIS Clock	Output Frequency 48 MHz Accuracy: ± 1% over the entire temperature range

LSI Clock	Output Frequency 114 kHz Accuracy: ± 4% over the entire temperature range
GPIO Input Clock	EXTCLK1/EXTCLK2/EXTCLK3/EXTCLK4， maximum supported input: 48 MHz

3.8.2 Clock Tree

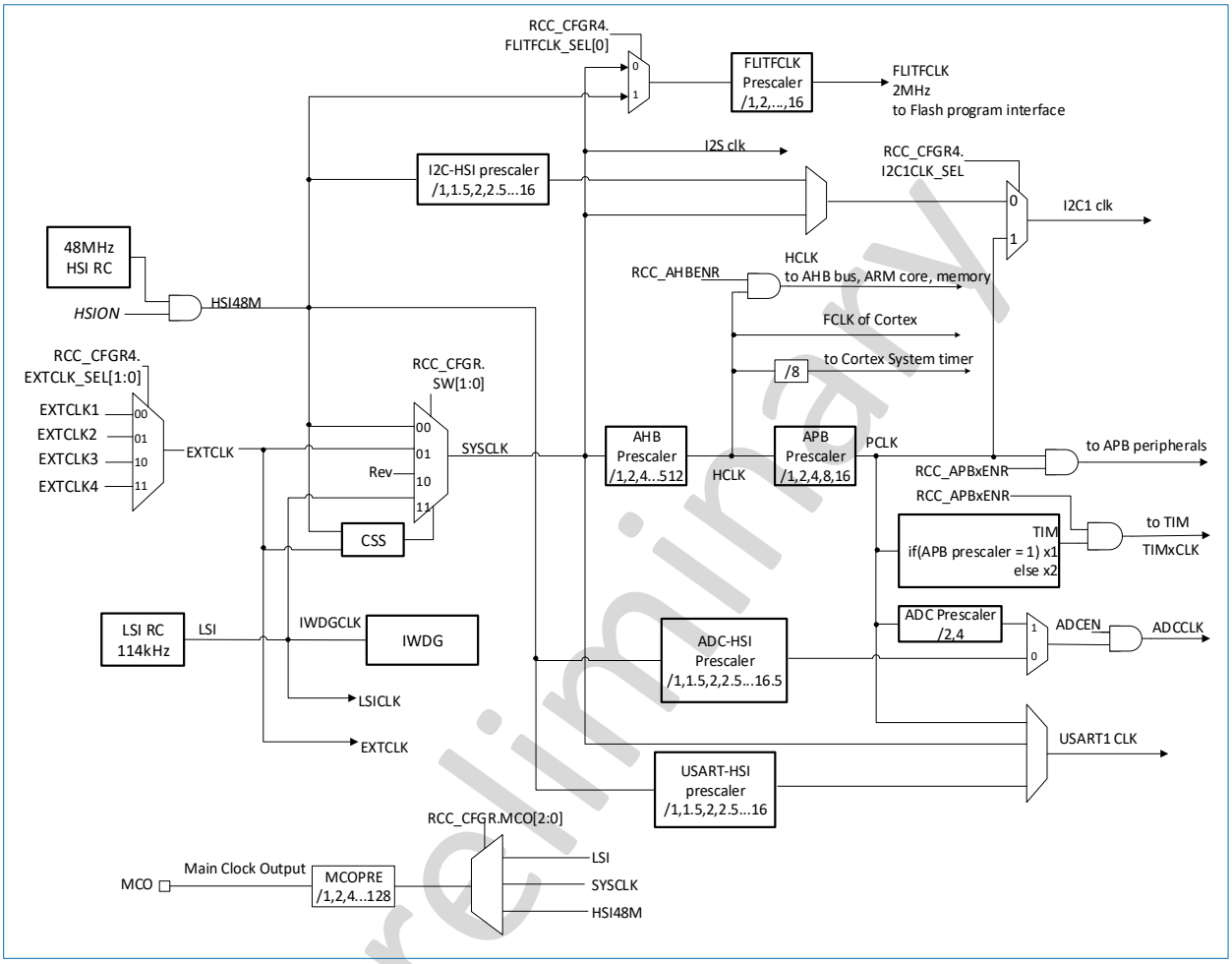

Figure 3-5 Clock Tree

- SYSCLK: Optional HSI48M, LSI, and GPIO input clocks, defaulting to HSI48M clock.
- HCLK: Default AHB pre-scaler is set to 6.
- FLITFCLK: Optional HSI48M and SYSCLK clocks.
- Adjustable GPIO input clock frequency threshold for CSS detection.

3.9 Power Supply

Scheme The PJ39900i-M0 MCU has three sets of power supplies: VIN, LDO5V, and VDD/VDDA. Among them, VIN provides input from 7 V – 24 V and outputs 5 V to the LDO5V pin. The LDO5V then supplies power to 3.3 V LDO and VDD/VDDA.

3.10 Low Power Mode

The PJ39900i-M0 MCU supports multiple power modes, achieving the optimal balance between low power consumption, short startup time, and various wake-up events.

- **Sleep Mode**

In sleep mode, only the CPU stops working while all peripherals remain active and can wake up the CPU upon interrupt/event occurrence.

- **Deep Sleep Mode**

In deep sleep mode, the system clock is lowered to 114 kHz to save power. In this mode, only the CPU stops working while all peripherals remain active and can wake up the CPU upon interrupt/event occurrence. The power consumption in deep sleep mode is higher than in stop mode.

- **Stop Mode**

While maintaining the contents of SRAM and registers, achieves the lowest energy consumption. In stop mode, all clocks in the core domain are disabled, and the HSI RC oscillator is turned off.

The MCU can be awakened from stop mode by configuring any signal as EXTI. This EXTI signal can be any external I/O port.

Table 3-6 Working Modes and Power Consumption

Working Modes	Power Consumption Metrics	Wake-up Time
Run Mode		-
Sleep Mode		21 ns
Deep Sleep Mode		Fastest 7.8 μs Wake-up
Stop Mode		10 μs

Low-power mode entry and wake-up conditions are as follows.

Table 3-7 Entry/Wake-up Conditions in Low-power Mode

Working Modes	Entry Conditions	Wake-up Conditions	Internal Core Power Clock Status	VDD Main Area Clock Status	Voltage Regulator Status
Sleep Mode	Setting PWR_CR: LPDS = 0; Software executes WFI/WFE instruction to enter.	Wake-up by any ordinary IRQ interrupt event, including System ticker.	CPU clock is turned off, no impact on other clocks and ADC clock.	Enabled	Enabled
Deep Sleep Mode	Switching the clock to LSI; Setting PWR_CR: LPDS = 0; Software executes WFI/WFE instruction to enter.	Wake-up by any ordinary IRQ interrupt event, including System ticker.	CPU clock is turned off, no impact on other clocks and ADC clock.	Enabled	Enabled

Working Modes	Entry Conditions	Wake-up Conditions	Internal Core Power Clock Status	VDD Main Area Clock Status	Voltage Regulator Status
Stop Mode	Setting PWR_CR: LPDS = 0; Setting the SLEEPDEEP bit of the CM0 system control register; Software executes WFI/WFE instruction to enter.	Supports wake-up by any EXTI external interrupt line. If entering Stop mode by executing WFI: set any external interrupt line to interrupt mode (the corresponding external interrupt vector must be enabled in NVIC). If entering Stop mode by executing WFE: set any external interrupt line to event mode. Supports Beeper-driven ADC sampling pre-wake-up. Actually wakes up when conditions are met. Supports Automatic Wake-up Timer (AWU) wake-up.	All clocks stop.	HSI turned off	Enabled or in low-power state (set in PWR_CR).

3.11 Independent Watchdog

The independent watchdog is powered by an internal independent 114 kHz RC oscillator, with a 12-bit decrement counter and an 8-bit pre-scaler. Because this RC oscillator operates independently of the main clock, it can run in standby mode. The IWDG can be used as a watchdog to reset the entire system in case of issues or as a free-running timer to provide timeout management for applications. Through the option byte field, it can be configured as a software or hardware-started watchdog. In debug mode, this counter can be frozen.

3.12 Window Watchdog

The window watchdog features a 7-bit decrement counter internally. This counter can be set to operate in free-running mode or as a watchdog to reset the entire system in the event of system crashes. The window watchdog is driven by the main clock and has early warning interrupt capabilities. In debug mode, this counter can be frozen.

3.13 System Tick Timer

The System Tick timer is dedicated to the operating system and serves as a standard decrement counter with the following features:

- 24-bit decrement counter
- Reload function
- Generates a mask able interrupt , when the counter reaches 0
- Programmable clock source

3.14 Basic Timer

The PJ39900i-M0 MCU integrates a basic timer, TIM6.

The basic timer features a built-in 16-bit counter, 16-bit pre-scaler, and supports up, down, or up/down counting modes. The basic timer is used to generate CPU timing interrupt requests. In debug mode, this counter can be frozen.

3.15 General-Purpose Timer

The PJ39900i-M0 MCU integrates one synchronize 4-channel general-purpose timer, TIM2.

The general-purpose timer can generate PWM outputs or serve as a simple time base. TIM2 features a 16-bit auto-reload up/down counter and a 16-bit pre-scaler. In debug mode, this counter can be frozen.

TIM2 can work in conjunction with advanced control timers through timer chaining, providing synchronization or event-linking capabilities, and can handle quadrature (incremental) encoder signals as well as digital outputs from 1 to 3 Hall effect sensors.

3.16 Advanced Timer

The PJ39900i-M0 MCU integrates an advanced timer, TIM1.

The advanced timer (TIM1) can function as a three-phase PWM generator with up to 6 channels allocated to it, and it can also serve as a complete general-purpose timer. Its four independent channels can be used for:

- Input capture
- Output compare
- PWM generation (edge-aligned or center-aligned mode)
- Single pulse output
- Complementary PWM output with programmable dead-time insertion.

When configured as a 16-bit basic timer, it shares the same functionality as the basic timer. Configured as a 16-bit PWM generator, it has full modulation capability (0 ~ 100%). Due to its similar internal structure and most functions to the general-purpose timer, the advanced timer can operate in conjunction with the general-purpose timer through timer chaining, providing synchronization or event linking functionality.

In debug mode, the counter can be frozen.

3.17 AWU Timer

The PJ39900i-M0 MCU integrates an Auto Wake-Up (AWU) timer. The AWU timer is used for timing during Stop mode and generating interrupts to wake up the MCU. It features an ultra-low-power 22-bit timer, and its working clock can be configured as 1 ~ 32 MHz GPIO input clock or 114 kHz on-chip slow clock (LSI). The AWU timer operates using a decrementing count method.

3.18 I2C Bus

A single I2C bus interface is capable of operating in master and slave modes, supporting standard, fast, and high-speed modes. The I2C interface supports 7-bit or 10-bit addressing, and in 7-bit slave mode, it supports dual slave address addressing. The I2C interface incorporates a hardware CRC generator/checker and supports SMBus V2.0/PMBus.

3.19 USART

The PJ39900i-M0 MCU features a built-in Universal Synchronous/Asynchronous Receiver Transmitter (USART), with a communication speed of up to 4 Mbit/s.

The USART supports multi-processor communication, host synchronous communication, and single-wire half-duplex communication mode. Additionally, the USART interface supports the ISO 7816 smart card communication protocol, IrDA SIR ENDEC specification, LIN master/slave function mode, and automatic baud rate detection feature.

The USART interface can utilize a clock domain independent of the CPU clock to wake up the MCU from Stop mode.

Table 3-8 USART Features

USART Mode/Features	USART
DMA Transmission	Not Supported
Multi-processor Communication	Supported
Synchronous Mode	Supported
Single-Wire Half-Duplex Communication	Supported
Dual Clock Domains and Wake-Up from Stop Mode	Supported
Automatic Baud Rate Detection	Supported
Modbus Communication	Supported
RS232 Hardware Flow Control	Not Supported
RS485 Driver Enable	Not Supported
IrDA SIR ENDEC Module	Supported
LIN Mode	Supported
Smart Card Mode	Supported

3.20 SPI

The PJ39900i-M0 MCU features 1 SPI interface, supporting communication speeds of up to 16 Mbit/s, and it accommodates both slave and master modes, as well as full-duplex and half-duplex communication modes. The SPI interface can utilize a 3-bit pre-scaler to generate 8 different master mode frequencies, and each frame can be configured for data lengths ranging from 4 to 16 bits.

The standard I2S interface (multiplexed with SPI) supports four different audio standards and is compatible with both master and slave half-duplex communication modes. The I2S interface is synchronized by dedicated signals and can be configured for 16-bit, 24-bit, or 32-bit transmission,

providing either 16-bit or 32-bit data resolution. The I2S interface's audio sampling frequency can be set from 8 kHz to 192 kHz using an 8-bit programmable linear pre-scaler. When operating in master mode, the I2S interface can output a clock that is 256 times the sampling frequency to external audio components.

Table 3-9 SPI Features

SPI Features	Is it supported
Hardware CRC Calculation	Supported
RX/TX FIFO	Supported
NSS Pulse Mode	Supported
I2S Mode	Supported
TI Mode	Supported

3.21 GPIO

Each GPIO pin can be configured by software as an output (push-pull or open-drain), input (floating, pull-up, or pull-down), or other peripheral function port. Most GPIO pins are shared with digital or analog peripherals. All GPIO pins have a high current passing capability. The peripheral function of I/O pins can be locked as needed to prevent accidental writing to I/O registers.

3.22 ADC

The ADC features of the PJ39900i-M0 MCU include:

- There are a total of 6 channels. Among them, AIN0 ~ AIN4 are external channel connections to IO, where AIN2 is connected to OP1 output pin, and AIN5 is an internal channel connected to internal reference voltage.
- Supports differential input mode, AIN0 and AIN1, AIN2 and AIN3 form two sets of differential inputs (when ADC is configured for differential input mode, the ADC channels of AIN4 and internal sampled BGR voltage are not available).
- Supports only 12-bit ADC sampling resolution.

3.22.1 External Trigger Source of ADC

Table 3-10 External Trigger Source of ADC

Name	Source	External Trigger Selection Mode（EXTSEL[2:0]）
TRG0	TIM1_TRGO	000
TRG1	TIM1_CC4	001
TRG2	TIM2_TRGO	010
TRG3	TIM6_TRGO	011
TRG4	TIM1_CC1	100
TRG5	TIM1_CC2	101
TRG6	TIM1_CC3	110
TRG7	IO_TRIG	111

IO_TRIG can be triggered by any IO, and users need to set the corresponding IO's MODER and AFR registers. For details, refer to the "GPIO Registers" section of the "MYg0002 User Manual."

3.22.2 AWD Wakeup Function

In Stop mode, the system can generate a signal to the ADC through the buzzer timer; the ADC captures this signal to wake up the ADC clock; after the ADC clock is ready, it triggers ADC conversion, generates AWD events based on ADC conversion results; AWD events output to EXTI can wake up the system.

Using this function, in addition to configuring the threshold and channel related to AWD, you also need to configure the ADC_CR2.WAKE_EN register, including the buzzer's internal corresponding timing control and the ADC's wakeup function enable register.

3.23 Operational Amplifiers

The chip has two built-in low offset operational amplifiers.

3.24 Built-in Drive

The chip integrates a three-phase brushless gate driver, used for driving MOSFETs in P+N structure. It incorporates a built-in undervoltage lockout (UVLO) function for input voltage VIN, effectively preventing the power transistors from operating at excessively low voltages. Additionally, it features built-in shoot-through prevention and dead time to prevent direct conduction of the driven high-side and low-side MOSFETs, effectively protecting the power device.

3.25 Input-Output Truth Table

The input pins LINx and HINx control the output states of LOx and HOx. The table below illustrates the logical relationship between inputs and outputs:

Table 3-11 Input-Output Logic Truth Table

LINx	HINx	LOx	HOx	Function
0	0	GND	VIN	External NMOS and PMOS both closed
0	1	GND	VIN-10V	External NMOS closed, PMOS open
1	0	10V	VIN	External NMOS open, PMOS closed
1	1	GND	VIN	External NMOS and PMOS both closed

3.25.1 Shoot-through Prevention Function

Internally designed specifically to prevent direct conduction of power transistors, the protection circuit effectively prevents damage to the power transistors caused by interference to the high-side and low-side input signals.

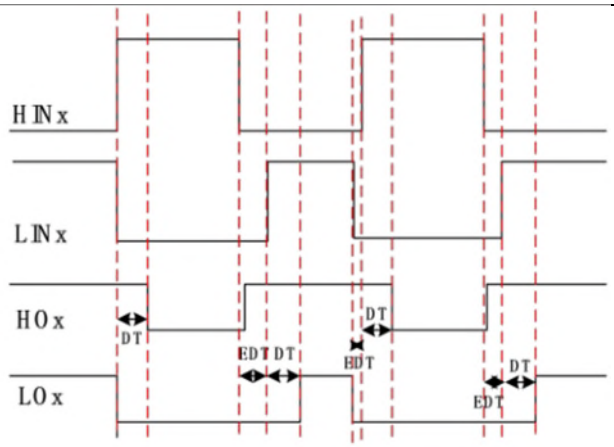

Figure 3-6 Shoot-through Prevention Function

3.25.2 Dead Time Function

A fixed dead time protection circuit is internally set. During the dead time, the high-side is set to a high level and the low-side output is set to a low level. The set dead time must ensure that one power transistor is turned off before another one is turned on, effectively preventing the occurrence of cross-conduction phenomena between the upper and lower power transistors. If an external dead time EDT is set for logical input, the dead time is equal to the external dead time EDT plus the internally set dead time DT.

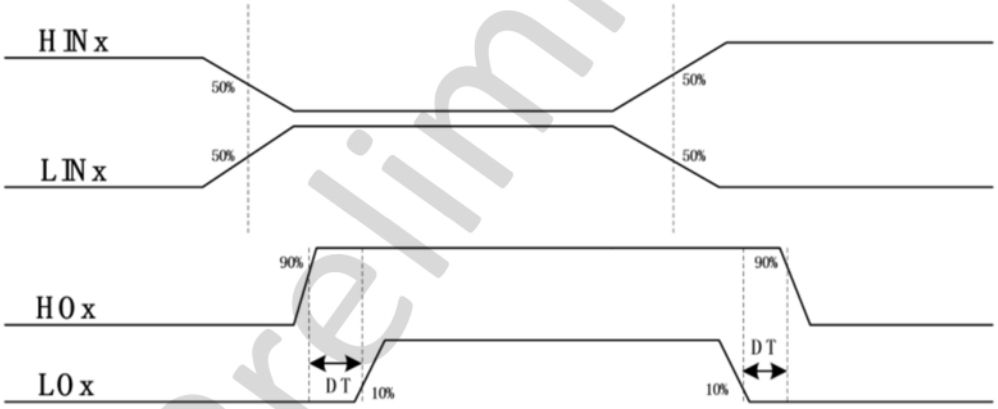

Figure 3-7 Dead Time

3.25.3 LDO

The chip integrates one 5V/50mA LDO and one 3.3V/50mA LDO.

3.26 MOSFET

The chip integrates three P+N mode half-bridge MOSFETs with smaller $R_{DS(ON)}$.

3.27 64-bit UID

The reference number provided by the 64-bit unique product identifier (UID) for any PJ39900i-M0 chip is unique in any circumstance. Users cannot modify this identifier. Depending on the usage, this 64-bit UID can be read in bytes (8 bits), half-words (16 bits), or full words (32 bits).

The 64-bit UID is suitable for the following applications:

- Used as a serial number (for example, USB character serial number or other terminal applications).
- Used as a password. When writing to flash memory, combining this UID with software encryption and decryption algorithms enhances the security of code stored in flash memory.
- Used to activate the bootstrapping process with security mechanisms.

3.28 Debug Interface

The chip embeds an ARM SWJ-DP interface, which combines the single-wire debug interface, enabling the connection of serial single-wire debug interfaces (SWDIO and SWCLK).

4 Electrical Characteristics

4.1 Power Supply

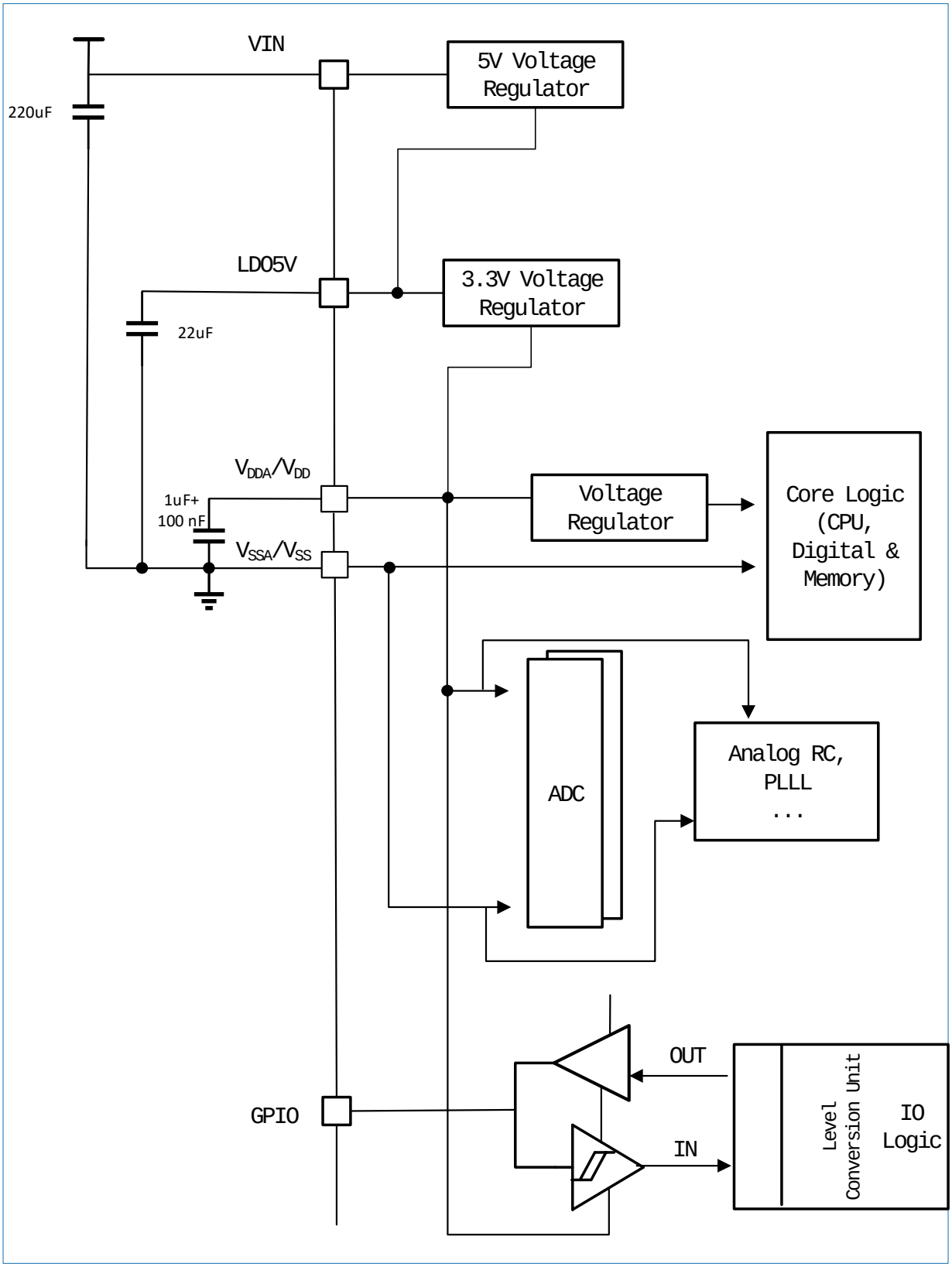

Figure 4-1 Power supply reference circuit

4.2 Maximum Absolute Ratings

The maximum rated value is only a short-term pressure value.

Notes:

- Do not operate the chip at this value or any other conditions exceeding the recommended values.
- Refer to Tables 4.1 to 4.18 for the maximum rated values of the chip. Exceeding the maximum rated values may result in permanent damage to the chip.
- Operating for prolonged periods at maximum rated values may affect the chip's reliability.

4.2.1 Limit Voltage Characteristics

Table 4-1 Limit Voltage Characteristics

Symbol	Description	Min.	Max.	Unit
V_{IN}	Voltage Range	6	40	V
$V_{INP1,2}$	Low Offset Operational Amplifier Positive Input Voltage Rang	-0.3	VLDO5V	
$V_{INN1,2}$	Low Offset Operational Amplifier Negative Input Voltage Range	-0.3	VLDO5V	
ESD	HBM	-	-	
	ESD	–	–	

4.2.2 Extreme Current Characteristics

Table 4-2 Extreme current characteristics

Symbol	Description	Max.	Unit
I_{VIN}	Maximum current flowing through VIN	5000	mA
I_{VDD}	Total current passing through VDD/VDDA power lines (supply current) (1)	150	
I_{VSS}	Total current passing through VSS ground lines (drain current) (1)	-	
I_{IO}	Output sinking current on any I/O and control pin	25	
	Output pulling current on any I/O and control pin	-25	
$I_{INJ(PIN)}$ (2)	Injection current on I/O pins (3)	±5	
$\Sigma_{IINJ(PIN)}$	Total injection current on all I/O and control pins (4)	±25	

(1). All power (VDD, VDDA) and ground (VSS, VSSA) pins must always be connected to an external power system within the allowed range.

(2). Reverse injection current may interfere with the device's analog performance.

(3). When VIN > VDD, there is a forward injection current; when VIN < VSS, there is a reverse injection current, and the injection current must not exceed the specified range.

(4). When multiple I/O ports have injection currents simultaneously, the maximum value of ∑IINJ (PIN) is the sum of the absolute values of the instantaneous forward and reverse injection currents.

4.2.3 Limit Temperature Characteristics

Table 4-3 Limit Temperature Characteristic

Symbol	Description	Reference Value	Unit
T_{STG}	Storage temperature range	-45 ~ +150	°C
T_J	Maximum junction temperature	125	

4.2.4 LDO Characteristics

Symbol	Description	Max.	Unit
V_{LDO5V}	5V LDO output / 3.3V LDO input	-	V
$V_{DD/VDDA}$	3.3V LDO output / MCU VDD input	-	
I_{LDO5V}	Maximum current output of 5V LDO	50	mA
$I_{LDO3.3V}$	Maximum current output of 3.3V LDO	50	

4.3 Operating Parameters

4.3.1 Recommended Operating Conditions

Table 4-4 Recommended Operating Condition

Symbol	Description	Min.	Typ.	Max.	Unit
V_{IN}	Power supply voltage range	7		24	V
I_{VIN}	Operating current of VIN		3000		mA
$V_{LDO5Vout}$(1)	5V LDO output voltage range	4.5		5.5	V
$I_{LDO5Vout}$	5V LDO output current range			50	mA
$V_{AO1,2}$(2)	Low-offset operational amplifier output voltage range	0		VLDO5V	V
$V_{INP1,2}$(2)	Low-offset operational amplifier positive input voltage range	0		VLDO5V	V
$V_{INN1,2}$(2)	Low-offset operational amplifier negative input voltage range	0		VLDO5V	V
$V_{LDO3.3Vout}$(3)	3.3V LDO output voltage range	3.23		3.36	V
$I_{LDO3.3Vout}$	3.3V LDO output current range			50	mA
f_{HCLK}	Internal AHB clock frequency	0		48	MHz
f_{PCLK}	Internal APB clock frequency	0		48	
P_D	Power consumption		-		W
T	Operating temperature	-40		85	°C

(1). $V_{LDO5Vout}$ internally connected with $V_{LDO3.3Vin}$, it is recommended to externally add filtering capacitors.

(2). When the operational amplifier output is directly connected to the MCU, $V_{AO1,2}$ / $V_{INP1,2}$ / $V_{INN1,2}$ are recommended to operate within the maximum range of $V_{LDO3.3Vout}$.

(3). V_{DD}、V_{DDA} and $V_{LDO3.3Vout}$ are internally merged on the chip, it is recommended to externally add filtering capacitors.

4.3.2 Reset and Low Voltage Detection

Table 4-5 Power-on Reset Characteristics

Symbol	Parameter	Condition	Min.	Typ.	Max.	Unit
T_{delay}	rstn setup time	-	-	40		μs
$V_{Threshold}$	Reset threshold	-	-	1.75		V

4.3.3 On/Off Reset Characteristics

Table 4-6 On/Off reset characteristics

Symbol	Parameter	Condition	Min.	Typ.	Max.	Unit
$V_{POR/PDR}$(1)	On/Off reset threshold	Falling edge(2)	1.8	1.88	1.96(3)	V
		Rising edge	1.84(3)	1.92	2.00	V
$V_{PDRhyst}$	PDR hysteresis	-	-	40	-	mV
$t_{RSTTEMPO}$(3)	Reset time	-	1.50	2.50	4.50	ms

(1) PDR/POR monitors V_{DD}/V_{DDA}。

(2) The measured values of the product are guaranteed to be lower than the minimum value of $V_{POR/PDR}$.

(3) Data are theoretical design values, not actual test values.

4.3.4 Internal Reference Voltage

Table 4-7 Internal Reference Voltage Characteristics

Symbol	Parameter	Condition	Min.	Typ.	Max.	Unit
V_{REFINT}	Internal Reference Voltage	-40 ~ 85°C	-	0.8	-	V

4.3.5 HIS Clock Characteristics

Table 4-8 HIS Characteristics

Symbol	Parameter	Condition	Min.	Typ.	Max.	Unit
f_{HSI}	Clock frequency	-	-	48	-	MHz
DuCy (HSI)	Duty cycle	-	45	-	55	%
ACC	Oscillator accuracy	User calibration of the RCC_CR register	-	-	1	
		Factory calibration, T_A= -40 ~ +85°C	-1	-	1	%
T_{su} (HSI)	Oscillator start-up time	$V_{SS} \le V_{IN} \le V_{DD}$	1	-	2	μs
I_{DD} (HSI)	Oscillator power consumption	-	-	80	100	μA

4.3.6 LSI Clock Characteristics

Table 4-9 LSI characteristics

Symbol	Parameter	Condition	Min.	Typ.	Max.	Unit
f_{LSI}	Clock frequency	-	-	114	-	kHz
$DuCy_{(LSI)}$	Duty cycle	-	45	-	55	%
ACC	Oscillator accuracy	Default: T_A=-40 ~+85 °C	1.5	-	2.2	
$T_{su(LSI)}$	Oscillator start-up time	$V_{SS} \le V_{IN} \le V_{DD}$	1	-	2	μs
$I_{DD(LSI)}$	Oscillator power consumption	-	-	5	8	μA

4.3.7 GPIO Input Clock

PJ39900i-M0 MCU supports clock input from EXTCLK1/EXTCLK2/EXTCLK3/EXTCLK4, with the following requirements :

Table 4-10 GPIO Input Clock

Symbol	Parameter	Min.	Typ.	Max.	Unit
Fext	Input clock frequency	1	8.0	32	MHz
	Input clock duty cycle	40	-	60	%
Jitter	Cycle Jitter	-	-	300	ps

4.3.8 Flash Memory Characteristics

Table 4-11 Flash Memory Characteristics

Symbol	Parameter	Min.	Typ.	Max.	Unit
T_{PROG}	Half-word write time	-	60	-	μs
T_{ERASE}	Page erase time	120	160	200	ms
	Chip erase time	120	160	200	ms
I_{DDPROG}	Half-word write current	-	-	5	mA
$I_{DDERASE}$	Page/chip erase current	-	-	2	mA
I_{DDREAD}	Read current @24MH	-	2	3	mA
	Read current @1MHz	-	0.25	0.4	mA
N_{END}	Write/erase endurance	100	-	-	千次
t_{RET}	Data retention time	10	-	-	年

4.3.9 IO Pin Input Characteristics

Table 4-12 IO Pin Straight Characteristics

Symbol	Parameter	Condition	Min.	Typ.	Max.	Unit
V_{IH}	Input high level	V_{DD} = 3.3 V	1.65 @ w/o Schmitt trigger 1.75 @ w/ Schmitt trigger	-	-	V

Symbol	Parameter	Condition	Min.	Typ.	Max.	Unit
V_{IL}	Input low level	V_{DD} = 3.3 V	-0.3	-	1.60 @ w/ Schmitt trigger 1.45 @ w/o Schmitt trigger	V
V_{hys}	Schmitt trigger voltage hysteresis	V_{DD} = 3.3 V	450	-	-	mV
I_{lkg}	Input leakage current	V_{IN} = 3.3 V	-	-	3	μA
R_{PU}	Pull-up resistor	V_{IN} = V_{SS}	30	40	50	KΩ
R_{PD}	Pull-down resistor	V_{IN} = V_{DD}	30	40	50	KΩ
C_{IO}	I/O pin capacitance		-	5	-	pF

4.3.10 IO Output Pin Characteristics

Table 4-13 IO Output Power Characteristics

Symbol	Parameter	Condition	Min.	Max.	Unit
V_{OL}	Output low level	V_{DD} = 3.3 V I_{OL} = -8 mA	0	0.8	V
V_{OH}	Output high level	V_{DD} = 3.3 V I_{OH} = 8 mA	2.4	3.3	
V_{OL}	Output low level	V_{DD} = 3.3 V I_{OL} = -20 mA	0	0.8	
V_{OH}	Output high level	V_{DD} = 3.3 V I_{OH} = 20 mA	2.4	3.3	

Table 4-14 IO AC Characteristics of Pin Output

Mode（MODER）	Symbol	Parameter	Condition	Min.	Max.	Unit
10	$f_{max(IO)out}$	Maximum frequency	C_L = 50 pF, V_{DD} = 2V ~ 3.6V	-	2	MHz
	$t_{f(IO)out}$	Fall time from output high to low level		-	125	ns
	$t_{r(IO)out}$	Rise time from output low to high level		-	125	
01	$f_{max(IO)out}$	Maximum frequency	C_L = 50 pF, V_{DD} = 2.7 V ~ 3.6 V	-	10	MHz
	$t_{f(IO)out}$	Fall time from output high to low level		-	25	ns
	$t_{r(IO)out}$	Rise time from output low to high level		-	25	
11	$f_{max(IO)out}$	Maximum frequency	C_L = 50 pF, V_{DD} = 2.7 V ~ 3.6 V	-	50	MHz
	$t_{f(IO)out}$	Fall time from output high to low level	C_L = 50 pF, V_{DD} = 2.7 V ~ 3.6 V	-	5	ns
	$t_{r(IO)out}$	Rise time from output low to high level	C_L = 50 pF, V_{DD} = 2.7 V ~ 3.6 V	-	5	ns

4.3.11 NRST Reset Pin Characteristics

The NRST pin is internally integrated with a pull-up resistor, and no external circuit is required in the peripheral application circuit. An RC circuit can be connected externally if needed.

Table 4-15 NRST Pin Input Characteristics

Symbol	Parameter	Min.	Max.	Unit
V_{IL}	NRST reset low-level voltage	-	0.8	V
V_{IH}	NRST input high-level voltage	2	-	V
V_{hys}	Schmitt trigger voltage	-	200	mV
R_{pull}	Internal weak pull-up resistor	-	50	K
T_{Noise}	Low-level is ignored	-	100	ns

4.3.12 TIM Counter Characteristics

Table 4-16 TIM Pin Input Characteristics

Symbol	Parameter	Min.	Max.	Unit
$t_{res(TIM)}$	Timer resolution time	1	-	$t_{TIMxCLK}$
f_{EXT}	External clock frequency for Timer CH1 to CH4	0	$F_{TIMxCLK}/2$ (1)	MHz
R_{ESTIM}	Timer resolution	-	16	Bit
$t_{counter}$	Clock period of the 16-bit counter when selecting the internal clock	1	65536	$t_{TIMxCLK}$
t_{MAX_COUNT}	Maximum possible count	-	65536 x 65536	$t_{TIMxCLK}$

(1). $f_{TIMxCLK}$ = 32 MHz

Table 4-17 TIM2 Pin Input Characteristics

Symbol	Parameter	Condition	Min.	Typ.	Max.	Unit
$t_{res（TIM）}$	Timer resolution time	$f_{TIMxCLK}$ = 32MHz	-	31.2	-	ns
f_{EXT}	Timer CH1 to CH4, external input clock frequency	-	-	$f_{TIMxCLK}/2$	-	MHz
		$f_{TIMxCLK}$ = 32MHz	-	16	-	MHz
t_{MAX_COUNT}	Clock period of the 16-bit counter when selecting the internal clock	-	-	216	-	$t_{TIMxCLK}$
		$f_{TIMxCLK}$ = 32MHz	-	2.048	-	ms

4.3.13 ADC Characteristics

Table 4-18 ADC Characteristics

Program	Description	Condition	Min.	Typ.	Max.	Unit
V_{DD}	ADC supply power	-	2	3.3	3.6	V
f_{ADC}	ADC clock frequency	-	0.6	-	14	MHz
f_S	Sampling frequency	-	0.05		1	MHz
f_{TRIG}	External trigger frequency	f_{ADC} = 14 MHz	-	-	823	kHz
		-	-		17	$1/f_{ADC}$
V_{AIN}	Conversion voltage range	-	0	-	VDD	V
R_{AIN}	External input impedance	-	-	-	50	kΩ

Program	Description	Condition	Min.	Typ.	Max.	Unit
R_{ADC}	Sampling switch resistance	-	-	-	1	kΩ
C_{ADC}	Sampling hold capacitor	-	-	-	5	pF
t_{CAL}	ADC calibration time	f_{ADC} = 14 MHz	5.9			μs
		-	8.3			$1/f_{ADC}$
t_{latr}	Regular trigger conversion delay	f_{ADC} = 14 MHz	-	-	0.143	μs
		-	-	-	2	$1/f_{ADC}$
t_S	Sampling time	f_{ADC} = 14 MHz	0.107	-	17.1	μs
		-	1.5	-	239.5	$1/f_{ADC}$
t_{STAB}	Power-on startup time	-	0	0	1	μs
t_{CONV}	Total conversion time (including sampling time)	f_{ADC} = 14 MHz	1	-	18	μs
		-	14 to 252 (ts + 12.5 used for successive approximation)			$1/f_{ADC}$
ADC 位数	12-bit (effective 8 bits)	-	-			-

4.3.14 Three-phase Gate Driver Characteristics

Table 4-19 Three-phase Gate Driver Characteristics

Parameter	Definition	Min.	Typ.	Max.	Unit
t_{DT}	Dead time	300	500	800	nS
T_{OTP}	Overheat protection threshold, turn off the entire chip		160		℃
T_{OTPHYS}	Overheat protection hysteresis		20		℃

4.3.15 Operational Amplifier Characteristics

Table 4-20 Operational Amplifier Characteristics

Parameter	Definition	Min.	Typ.	Max.	Unit
V_{OP}	Operational amplifier operating voltage		5		V
V_{OFFSET}	Offset voltage		3	7	mV
V_{CRANGE}	Input common-mode voltage range	0		V_{OP}-0.2	V
I_{IN}	Input bias current			1	uA
I_{SOURCE}	Output sourcing current	1000			uA
I_{SINK}	Output sinking current	1000			uA
V_{SW}	Output voltage swing	0		V_{OP}	V
Slew rate	Rising edge		8.5		V/us
	Falling edge		5		V/us
Av	Open-loop achievement		10		Kv/V
BW	Bandwidth		6		MHZ

4.3.16 N-MOS Electrical Characteristics

Table 4-21 N-MOS Electrical Characteristics

Symbol	Description	Condition	Min.	Typ.	Max.	Unit
Cut-off characteristics						
B_{VDSS}	Drain-source breakdown voltage	V_{GS} = 0 V, I_D = 250 μA	40	-	-	V
I_{DSS}	Leakage current with gate-source short	V_{DS} = 40 V, V_{GS} = 0 V	-	-	1	μA
I_{GSS}	Gate current with drain-source short	V_{DS} = 0 V, V_{GS}= ±20 V	-	-	±100	nA
Conduction characteristics						
$V_{GS(th)}$	Gate-source threshold voltage	V_{DS} = V_{GS}, I_D = 250 μA	1.0	1.35	2.0	V
$R_{DS(ON)}$	Drain-source on-state resistance	-	-	-	-	mΩ
gfs	Transconductance	V_{DS} = 5 V, I_D = 1 A	-	15	-	S
Switching characteristics						
$t_{D(ON)}$	Turn-on delay time	V_{DS} = 20 V V_{GS} = 10 V R_L = 1.8 Ω R_{GEN} = 3 Ω	-	4	-	nS
tr	Rise time		-	3	-	
$t_{D(OFF)}$	Turn-off delay time		-	15	-	
tf	Fall time		-	2	-	

4.3.17 P-MOS Electrical Characteristics

Table 4-22 N-MOS Electrical Characteristics

Symbol	Description	Condition	Min.	Typ.	Max.	Unit
Cut-off characteristics						
B_{VDSS}	Drain-source breakdown voltage	V_{GS} = 0 V, I_D = -250 μA	-40	-	-	V
I_{DSS}	Leakage current with gate-source short	V_{DS} = -40 V, V_{GS} = 0 V	-	-	-1	μA
I_{GSS}	Gate current with drain-source short	V_{DS} = 0 V, V_{GS} = ±20 V	-	-	±100	nA
Conduction characteristics						
$V_{GS(th)}$	Gate-source threshold voltage	V_{DS} = V_{GS}, I_D = -250 μA	-1.0	-1.35	-2.0	V
$R_{DS(ON)}$	Drain-source on-state resistance	-	-		-	mΩ
gfs	Transconductance	V_{DS} = -5 V, I_D = -1 A	-	18	-	S
Switching characteristics						
$t_{D(ON)}$	Turn-on delay time	V_{DS} = 20 V V_{GS} = 10 V R_L = 2.3 Ω R_{GEN} = 3 Ω	-	10	-	nS
tr	Rise time		-	5.5	-	
$t_{D(OFF)}$	Turn-off delay time		-	3.6	-	
tf	Fall time		-	4.6	-	

5 Pin Definition

PJ39900i-M0 MCU uses TSSOP-25P package, with the following pin definitions.

5.1 TSSOP-25P Package

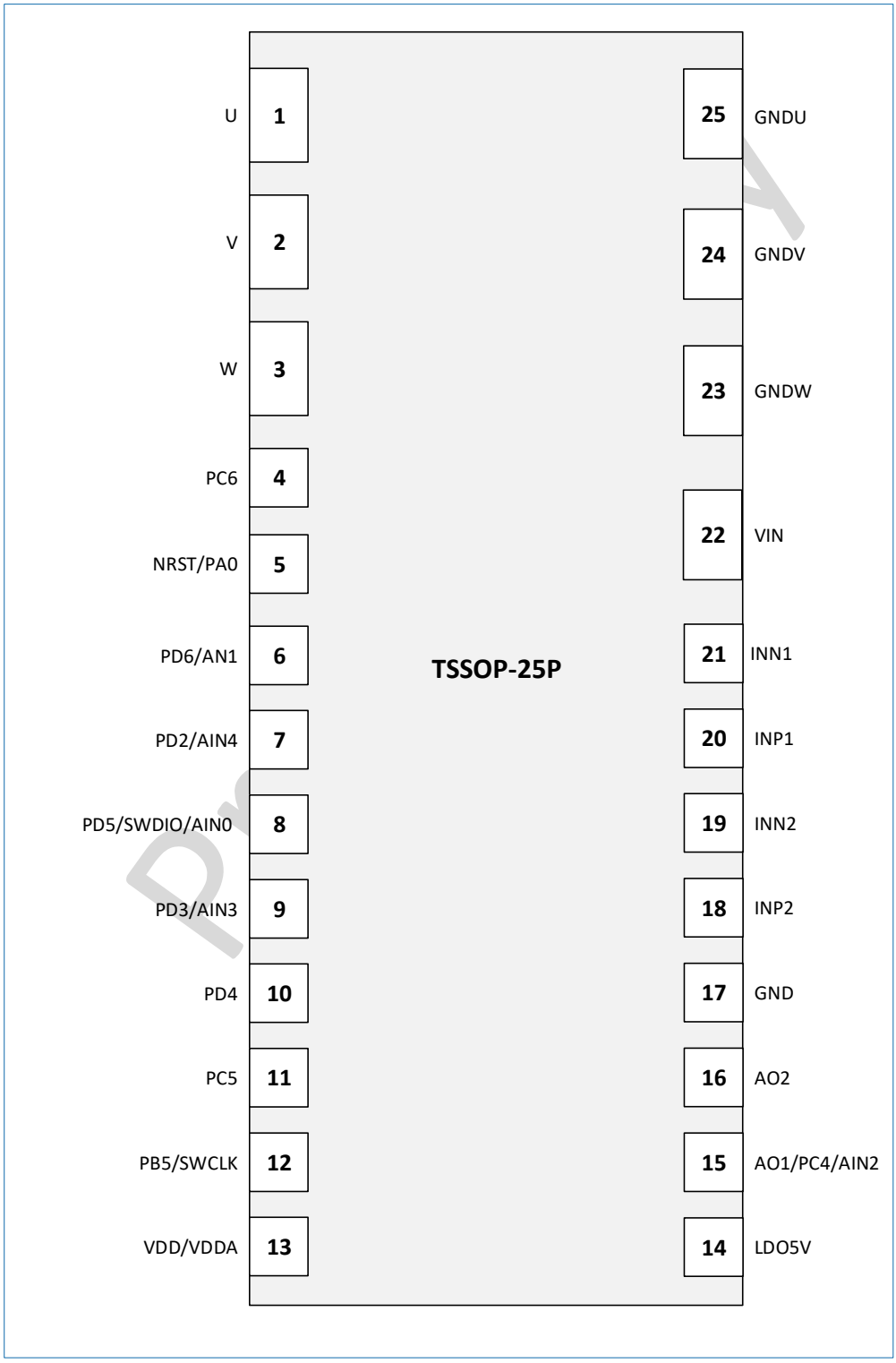

Figure 5-1 TSSOP-25P Package

Table 5-1 Pin Definitions for TSSOP-25P Package

Pin Number	Pin Name	Pin Type (1)	Default Pin Function after Power-On	Default Multiplexed Pin Function (AF0)
1	U	O	Phase U Output	
2	V	O	Phase V Output	
3	W	O	Phase W Output	
4	PC6	I/O	PC6	-
5	NRST/PA0	I/O	NRST	-
6	PD6/AIN1	I/O	PD6	-
7	PD2/AIN4 (2)	I/O	PD2	-
8	PD5/SWDIO/AIN0 (2)	I/O	SWDIO	SWDIO
9	PD3/AIN3 (2)	I/O	PD3	-
10	PD4	I/O	PD4	I2C_SMBA
11	PC5/EXTCLK4	I/O	PC4/ PC5	I2C_SDA
12	PB5/SWCLK/EXTCLK3	I/O	SWCLK	SWCLK_I2C_SDA(3)
13	VDD/VDDA	S	Chip's digital and analog supplies are connected	
14	LDO	O	5V LDO output, with an external 1uF capacitor to ground	
15	AO1/PC4/AIN2(2)	I/O	Output of Low Offset Op-Amp for Channel 1, Analog Channel 2 input	
16	AO2	O	Output of Low Offset Op-Amp for Channel 2	
17	VSS/VSSA	S	Chip's digital ground and analog ground are connected	
18	INP2	I	Positive input of Low Offset Op-Amp for Channel 2	
19	INN2	I	Negative input of Low Offset Op-Amp for Channel 2	
20	INP1	I	Positive input of Low Offset Op-Amp for Channel 1	
21	INN1	I	Negative input of Low Offset Op-Amp for Channel 1	
22	VIN	PWR	Input power supply, with an external 1uF capacitor to ground	
23	GNDW	S	W Phase Ground	
24	GNDV	S	V Phase Ground	
25	GNDU	S	V Phase Ground	

"I" represents input, "O" represents output, "I/O" represents input/output, "S" represents power supply.

(1). AIN0 ~ AIN4 have ADC analog input function.

(2). PB5 requires additional configuration register to select SWCLK or I2C_SDA.

5.2 Pin Multiplexing (AF) Function Table

Table 5-2 Pin Multiplexing Function Table

Pin Name	AF0 (I2C/SWD)	AF1 (USART)	AF2 (SPI/I2S)	AF3 (TIM1)	AF4 (TIM2)	AF5 (RCC)	AF6 (Beeper)	AF7 (ADC)
PA0	Reserved	Reserved	Reserved	TIM1_BKIN	TIM2_CH3	RCC_MCO	BEEP	ADC_ETR
PA1	Reserved	Reserved	Reserved	TIM1_CH1N	TIM2_ETR	RCC_MCO	BEEP	ADC_ETR
PA2	I2C_SMBA	Reserved	SPI_SCK/ I2S_CK	TIM1_CH2N	TIM2_CH4	RCC_MCO	BEEP	ADC_ETR
PA3	Reserved	USART_TX	SPI_NSS/ I2S_WS	TIM1_CH3N	TIM2_CH3	RCC_MCO	BEEP	ADC_ETR
PB4	I2C_SCL	USART_RX	SPI_MISO/ I2S_MCK	TIM1_CH2N	TIM2_ETR	RCC_MCO	BEEP	ADC_ETR
PB5	SWCLK_I2C_ SDA (1)	USART_RX	SPI_NSS/ I2S_WS	TIM1_BKIN	TIM2_CH2	RCC_MCO	BEEP	ADC_ETR
PC3	Reserved	USART_CK	Reserved	TIM1_CH3_ CH1N (2)	TIM2_CH1	RCC_MCO	BEEP	ADC_ETR
PC4	Reserved	Reserved	SPI_MISO/ I2S_MCK	TIM1_CH4_ CH2N (2)	TIM2_CH4	RCC_MCO	BEEP	ADC_ETR
PC5	I2C_SDA	Reserved	SPI_SCK/ I2S_CK	TIM1_ETR	TIM2_CH1	RCC_MCO	BEEP	ADC_ETR
PC6	I2C_SCL	Reserved	SPI_MOSI/ I2S_SD	TIM1_CH1	TIM2_CH3	RCC_MCO	BEEP	ADC_ETR
PC7	Reserved	Reserved	SPI_MISO/ I2S_MCK	TIM1_CH2	TIM2_ETR	RCC_MCO	BEEP	ADC_ETR
PD1	I2C_SMBA	USART_TX	Reserved	TIM1_CH1	TIM2_CH4	RCC_MCO	BEEP	ADC_ETR
PD2	Reserved	Reserved	SPI_MOSI/ I2S_SD	TIM1_CH2	TIM2_CH3	RCC_MCO	BEEP	ADC_ETR
PD3	Reserved	Reserved	SPI_SCK/ I2S_CK	TIM1_CH3	TIM2_CH2	RCC_MCO	BEEP	ADC_ETR
PD4	I2C_SMBA	USART_CK	SPI_MOSI/ I2S_SD	TIM1_CH4	TIM2_CH1	RCC_MCO	BEEP	ADC_ETR
PD5	SWDIO	USART_TX	Reserved	TIM1_ETR	TIM2_ETR	RCC_MCO	BEEP	ADC_ETR
PD6	Reserved	USART_RX	SPI_MISO/ I2S_MCK	TIM1_CH2	TIM2_CH2	RCC_MCO	BEEP	ADC_ETR
PD7	I2C_SMBA	USART_RX	SPI_NSS/ I2S_WS	TIM1_CH3	TIM2_CH1	RCC_MCO	BEEP	ADC_ETR

(1). PB5 requires configuration of IOMUX peripheral registers to select SWCLK or I2C_SDA.

(2). PC3 and PC4 require configuration of IOMUX peripheral registers to select TIM1's CH3/CH4 or CH1N/CH2N.

bit	2	1	0
	PB5_I2C1_SEL	PC4_TIM1_SEL	PC3_TIM1_SEL
access	rw	rw	rw
reset value	0	0	0

Figure 5-2 Multiplexing Function Selection for PB5/PC4/PC3

- **If PB5_AF is configured as AF0, when PB5_I2C_SEL value is:**
  - 0: PB5 functions as SWCLK input pin (default setting during system reset).
  - 1: PB5 functions as I2C SDA pin.
- **If PC4_AF is configured as AF3, when PC4_TIM1_SEL value is:**
  - 0: PC3 functions as TIM1's CH4 pin.
  - 1: PC3 functions as TIM1's CH2N pin.
- **If PC3_AF is configured as AF3, when PC3_TIM1_SEL value is:**
  - 0: PC3 functions as TIM1's CH3 pin.
  - 1: PC3 functions as TIM1's CH1N pin.

6 Package Parameter

6.1 Package Size

6.1.1 TSSOP-25P Package

Package Size is 9.70 mm x 4.40 mm for TSSOP-25P.

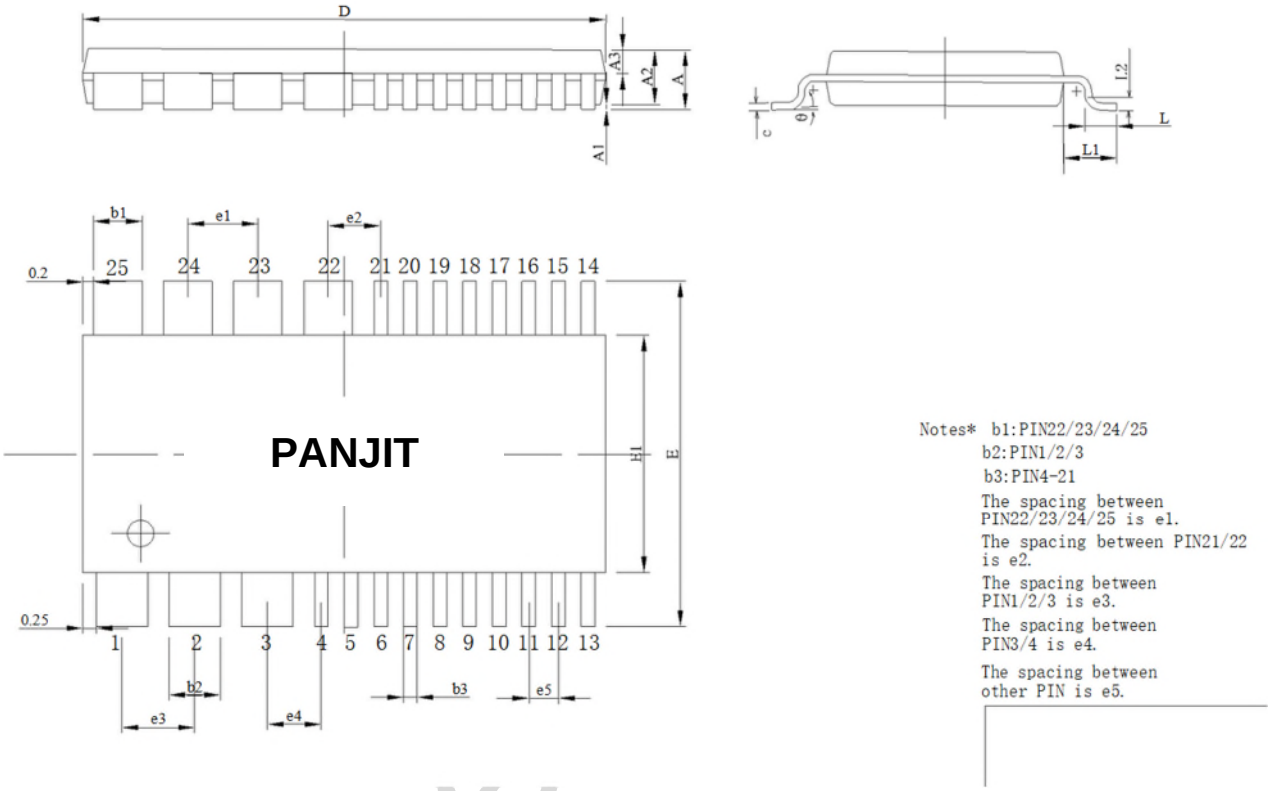

Figure 6-1 TSSOP-25P Package Size

Table 6-1 TSSOP-25P Package Size Parameter

Symbol	Min.（mm）	Typ.（mm）	Max.（mm）
A	-	-	1.2
A1	0.03	0.08	0.12
A2	0.80	-	1.0
A3	0.39	0.44	0.49
b1	-	0.90	-
b2	-	0.05	-
b3	-	0.25	-
c	0.14	-	0.18
D	9.60	9.70	9.80
E	6.20	6.40	6.60
E1	4.30	4.40	4.50
e1	1.3BSC		

Symbol	Min.（mm）	Typ.（mm）	Max.（mm）
e2	0.98BSC		
e3	1.35BSC		
e4	1.0BSC		
e5	0.55BSC		
L	0.45	0.60	0.75
L1	1.0BSC		
L2	0.25BSC		
θ	0	-	8°

6.1.2 Silkscreen Information

The silkscreen information includes the Element Energy logo, product model, and product batch number. The explanation of the product batch number is shown in the following table.

Table 6-2 Product Batch Number Explanation

Product Batch Number	Explanation
Character 1	Represents the packaging factory
Character 2	Represents the year, for example, 3 represents the year 2023
Character 3 and 4	- Represent the week, for example, 26 represents the 26th week
Character 5、6 and 7	Represent the last three digits of the wafer batch number
Character 8 and 9	Version number

7 Ordering Information

7.1 Ordering Packaging

Table 7-1 Product Ordering Packaging

Package	Specific Model	Packaging	Remarks
TSSOP-25P	PJ39900i-M0	Tape Reel	

8 Acronyms

Acronyms	Full Name	Description in Chinese
ADC	Analog-to-Digital Converter	模拟数字转换器
AHB	Advanced High-Performance Bus	高级高性能总线
APB	Advanced Peripheral Bus	外围总线
AWU	Auto-Wakeup	自动唤醒
CRC	Cyclic Redundancy Check	循环冗余校验码
CSS	Clock Security System	时钟安全系统
DMA	Direct Memory Access	直接存储器访问
EEPROM	Electrically Erasable Programmable Read Only Memory	电可擦编程只读存储器
EXTI	Extended Interrupts and Events Controller	中断和事件控制器
GPIO	General Purpose Input Output	通用输入输出
I2C	Inter-Integrated Circuit	I2C 总线
I2S	Inter-IC Sound	I2S 总线
IWDG	Independent Watchdog	独立看门狗
LSI	Low-Speed Internal（Clock Signal）	低速内部（时钟信号）
MCU	Microcontroller Unit	微控制单元
MSPS	Million Samples Per Second	每秒百万次采样
NVIC	Nested Vectored Interrupt Controller	嵌套矢量中断控制器
PDR	Power-Down Reset	掉电复位
PLL	Phase Locked Loop	锁相环
POR	Power-On Reset	上电复位
PWM	Pulse Width Modulation	脉宽调制
RCC	Reset and Clock Control	复位时钟控制
RISC	Reduced Instruction Set Computing	精简指令集计算机
SPI	Serial Peripheral Interface	串行外设接口
SRAM	Static Random Access Memory	静态随机存储器
SWD	Serial Wire Debug	串行线调试
USART	Universal Synchronous Asynchronous Receiver Transmitter	通用同步/异步收发器
WWDG	Window Watchdog	窗口看门狗

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