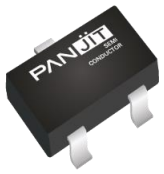
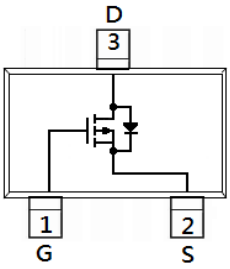
PJA3461S-AU

60V P-Channel Enhancement Mode MOSFET

Voltage	-60 V	Current	-1.9 A

SOT-23





Features

- $R_{DS(ON)}$, V_{GS}@-10V, I_D@-1.9A<200mΩ
- $R_{DS(ON)}$, V_{GS}@-4.5V, I_D@-1.5A<270mΩ
- Advanced Trench Process Technology
- Specially Designed for Switch Load, PWM Application, etc
- AEC-Q101 qualified
- Lead free in compliance with EU RoHS 2.0
- Green molding compound as per IEC 61249 standard

Mechanical Data

- Case : SOT-23 Package
- Terminals : Solderable per MIL-STD-750, Method 2026
- Approx. Weight : 0.0084 grams

Maximum Ratings and Thermal Characteristics (T_A=25°C unless otherwise noted)

PARAMETER		SYMBOL	LIMIT	UNITS
Drain-Source Voltage		V_{DS}	-60	V
Gate-Source Voltage		V_{GS}	±20	
Continuous Drain Current(Note 3)	T_A=25°C	I_D	-1.9	A
	T_A=70°C		-1.6	
Pulsed Drain Current(Note 1)	T_A=25°C	I_{DM}	-7.6	
Power Dissipation	T_A=25°C	P_D	1.5	W
	T_A=70°C		1.05	
Operating Junction and Storage Temperature Range		T_J,T_{STG}	-55~175	°C
Thermal Resistance(Note 3,4)	Junction to Ambient	$R_{\theta JA}$	100	°C/W

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Electrical Characteristics (T_A=25°C unless otherwise noted)

PARAMETER	SYMBOL	TEST CONDITION	MIN.	TYP.	MAX.	UNITS
Static						
Drain-Source Breakdown Voltage	BV_{DSS}	V_{GS}=0V, I_D=-250uA	-60	-	-	V
Gate Threshold Voltage	$V_{GS(th)}$	V_{DS}=V_{GS}, I_D=-250uA	-1	-1.7	-2.5	
Drain-Source On-State Resistance	$R_{DS(on)}$	V_{GS}=-10V, I_D=-1.9A	-	160	200	mΩ
		V_{GS}=-4.5V, I_D=-1.5A	-	204	270	
Zero Gate Voltage Drain Current	I_{DSS}	V_{DS}=-60V, V_{GS}=0V	-	-	-1	uA
Gate-Source Leakage Current	I_{GSS}	V_{GS}=±20V, V_{DS}=0V	-	-	±100	nA
Dynamic(Note 5)						
Total Gate Charge	Q_g	V_{DS}=-30V, I_D=-1.9A, V_{GS}=-10V(Note 2)	-	9	13	nC
Gate-Source Charge	Q_{gs}		-	1.5	-	
Gate-Drain Charge	Q_{gd}		-	1.5	-	
Input Capacitance	Ciss	V_{DS}=-30V, V_{GS}=0V, f=1MHz	-	340	510	pF
Output Capacitance	Coss		-	27	50	
Reverse Transfer Capacitance	Crss		-	17	30	
Gate resistance	R_g	f=1MHz	-	14.4	-	Ω
Turn-On Delay Time	$td_{(on)}$	V_{DS}=-30V, I_D=-1.9A, V_{GS}=-10V, R_G=6Ω(Note 1,2)	-	3.6	-	ns
Turn-On Rise Time	t_r		-	2.9	-	
Turn-Off Delay Time	$td_{(off)}$		-	19	-	
Turn-Off Fall Time	t_f		-	8	-	
Drain-Source Diode						
Diode Forward Current	I_S	T_C=25°C	-	-	-1.9	A
Pulsed Diode Forward Current	I_{SM}		-	-	-7.6	
Diode Forward Voltage	V_{SD}	I_S=-1A, V_{GS}=0V	-	-0.8	-1	V
Reverse Recovery Time	Trr	V_{DD}=-30V,V_{GS}=0V, I_S=-1.9A,dI_S/dt=100A/us	-	9	-	ns
Reverse Recovery Charge	Qrr		-	5	-	nC

NOTES :

1. Pulse width≤300us, Duty cycle≤2%.
2. Essentially independent of operating temperature typical characteristics.
3. Chip capability with an $R_{\theta JA}$=100°C/W.
4. $R_{\theta JA}$ is the sum of the junction-to-case and case-to-ambient thermal resistance where the case thermal reference is defined as the solder mounting surface of the drain pins. Mounted on a 1 inch^2 with 2oz.square pad of copper.
5. Guaranteed by design, not subject to production testing.

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TYPICAL CHARACTERISTIC CURVES

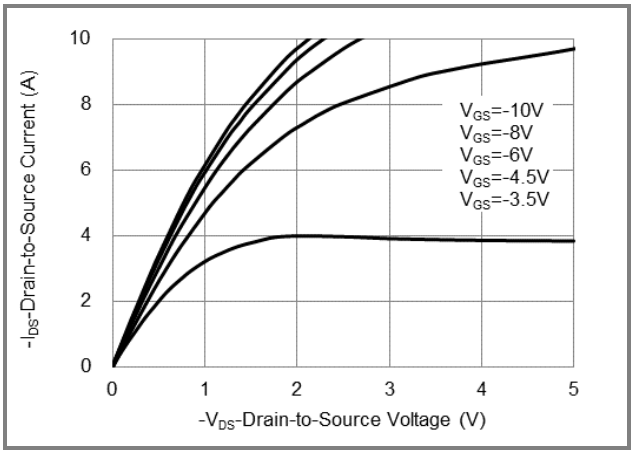

Fig.1 On-Region Characteristics

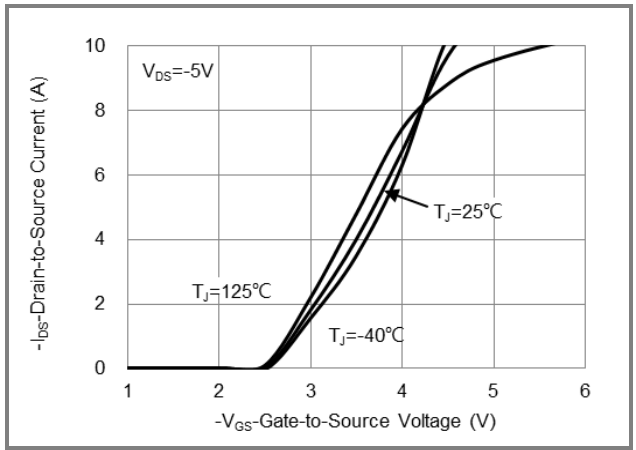

Fig.2 Transfer Characteristics

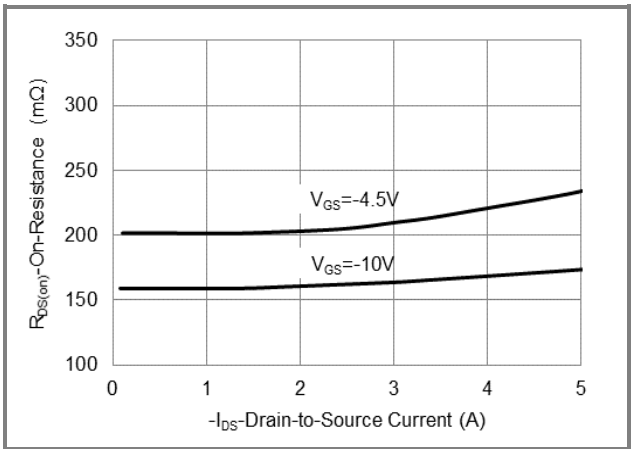

Fig.3 On-Resistance vs. Drain Current

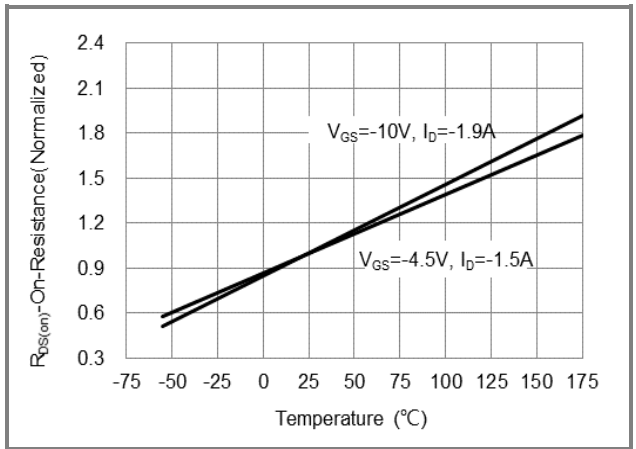

Fig.4 On-Resistance vs. Junction temperature

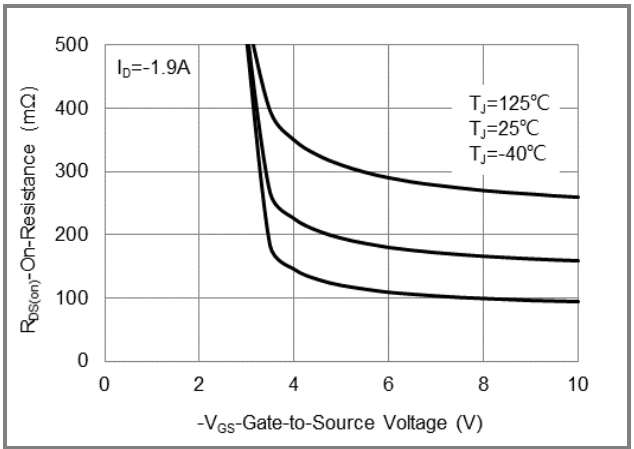

Fig.5 On-Resistance Variation with V_{GS}

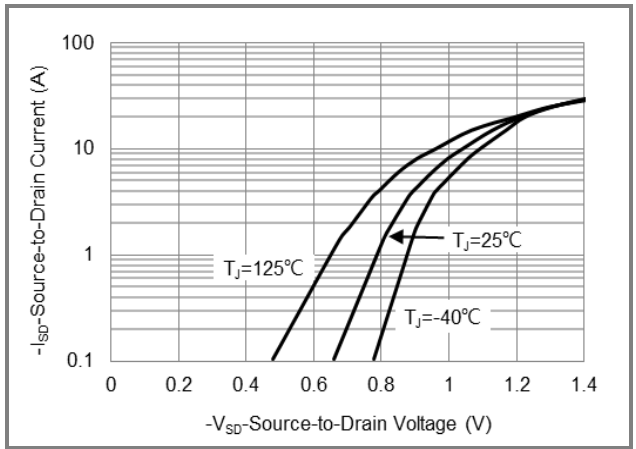

Fig.6 Source-Drain Diode Forward Voltage

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TYPICAL CHARACTERISTIC CURVES

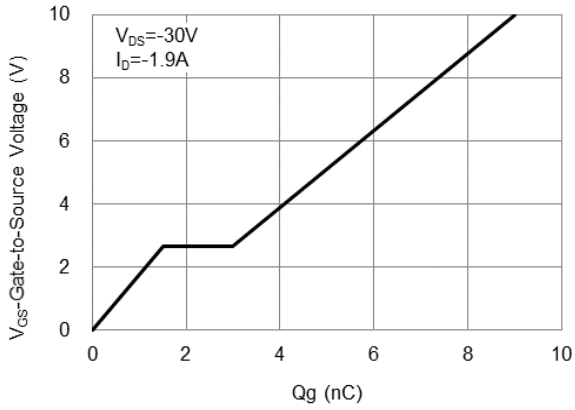

Fig.7 Gate-Charge Characteristics

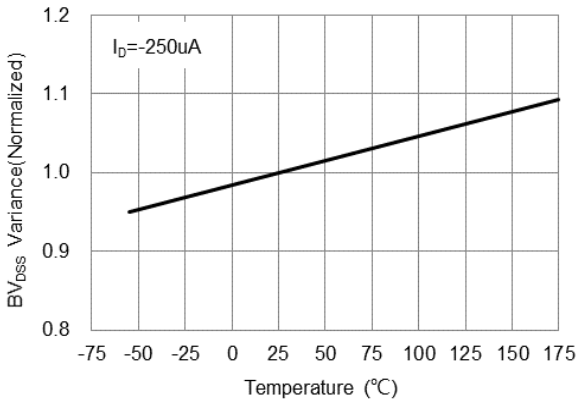

Fig.8 Breakdown Voltage Variation vs. Temperature

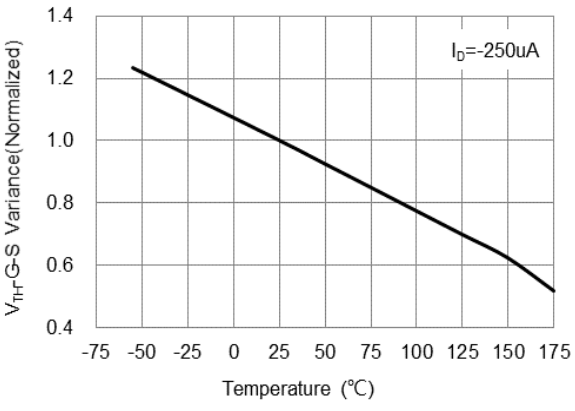

Fig.9 Threshold Voltage Variation with Temperature

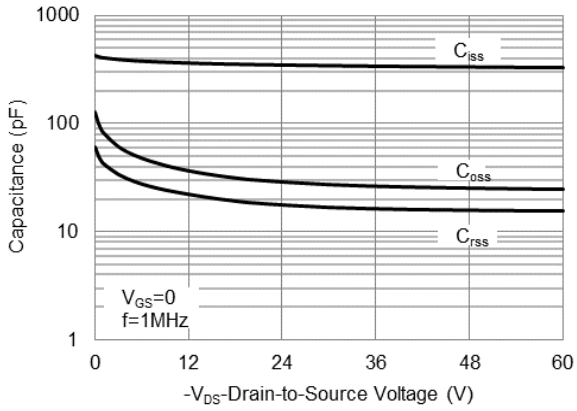

Fig.10 Capacitance vs. Drain-Source Voltage

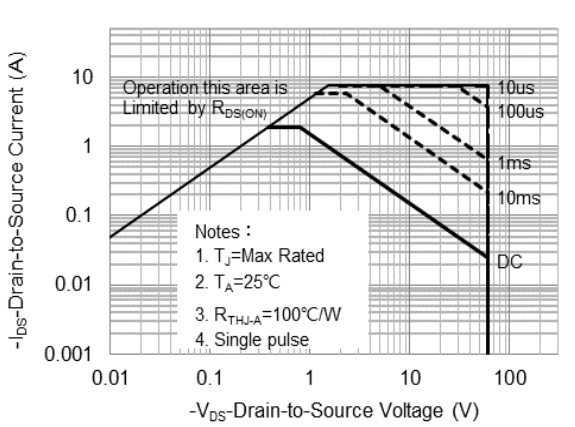

Fig.11 Maximum Safe Operating Area

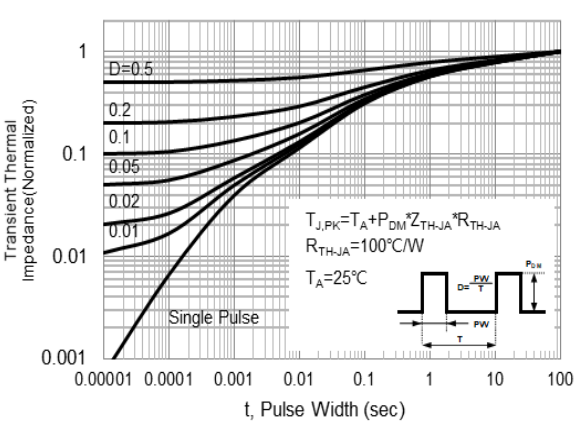

Fig.12 Normalized Transient Thermal Impedance

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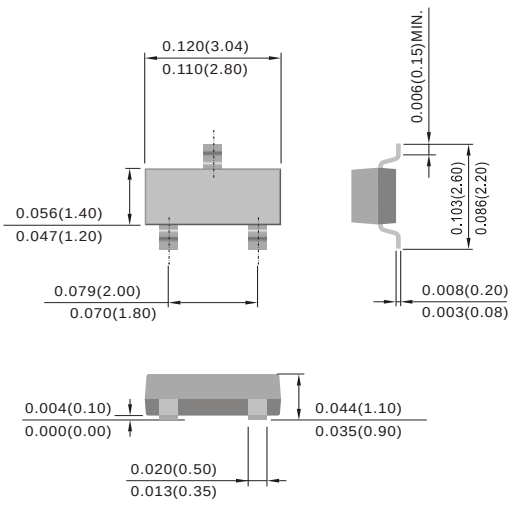
Product and Packing Information

Part No.	Package Type	Packing Type	Marking
PJA3461S-AU	SOT-23	3K pcs / 7” reel	61S

Packaging Information & Mounting Pad Layout

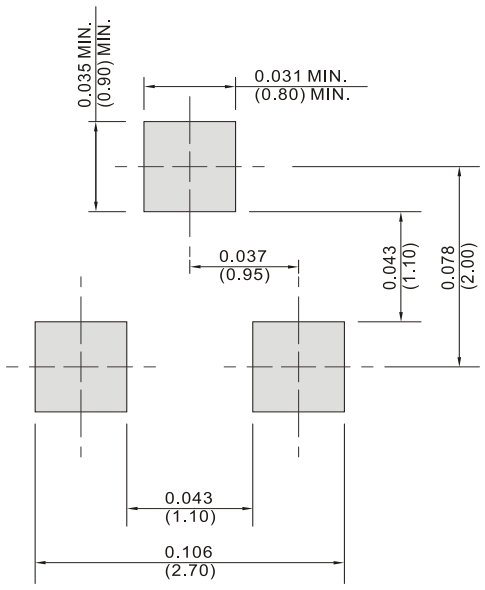
SOT-23 Dimension

Unit: inch(mm)



SOT-23 Pad Layout

Unit: inch(mm)



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