

PJQ24611AW-AU

60V P-Channel Enhancement Mode MOSFET

Voltage **-60 V** **Current** **-14 A**

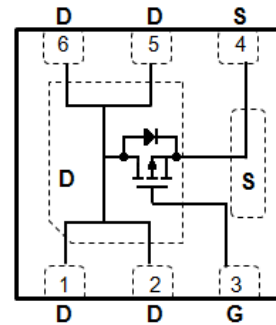
Features

- $R_{DS(ON)}$, $V_{GS}@-10V$, $I_D@-4A < 85m\Omega$
- $R_{DS(ON)}$, $V_{GS}@-4.5V$, $I_D@-2A < 115m\Omega$
- Excellent FOM
- Wettable flank terminals
- AEC-Q101 qualified
- Lead free in compliance with EU RoHS 2.0
- Green molding compound as per IEC 61249 standard

Mechanical Data

- Case : DFN2020BW-6L Package
- Terminals : Solderable per MIL-STD-750, Method 2026
- Approx. Weight : 0.0096 grams

DFN2020BW-6L



Maximum Ratings and Thermal Characteristics ($T_A=25^\circ\text{C}$ unless otherwise noted)

PARAMETER		SYMBOL	LIMIT	UNIT
Drain-Source Voltage		V_{DS}	-60	V
Gate-Source Voltage		V_{GS}	± 20	
Continuous Drain Current ^(Note 3)	$T_C=25^\circ\text{C}$	I_D	-14	A
	$T_C=100^\circ\text{C}$		-10	
Pulsed Drain Current ^(Note 1)	$T_C=25^\circ\text{C}$	I_{DM}	-24	
Power Dissipation	$T_C=25^\circ\text{C}$	P_D	36	W
	$T_C=100^\circ\text{C}$		18	
Continuous Drain Current ^(Note 4)	$T_A=25^\circ\text{C}$	I_D	-3.8	A
	$T_A=70^\circ\text{C}$		-3.1	
Power Dissipation	$T_A=25^\circ\text{C}$	P_D	2.4	W
	$T_A=70^\circ\text{C}$		1.7	
Operating Junction and Storage Temperature Range		T_J, T_{STG}	-55~175	$^\circ\text{C}$
Thermal Resistance ^(Note 4)	Junction to Case	$R_{\theta JC}$	4.1	$^\circ\text{C/W}$
	Junction to Ambient	$R_{\theta JA}$	62.5	

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Electrical Characteristics (T_A=25°C unless otherwise noted)

PARAMETER	SYMBOL	TEST CONDITION	MIN.	TYP.	MAX.	UNIT
Static						
Drain-Source Breakdown Voltage	BV _{DSS}	V _{GS} =0V, I _D =-250uA	-60	-	-	V
Gate Threshold Voltage	V _{GS(th)}	V _{DS} =V _{GS} , I _D =-250uA	-1	-1.7	-2.5	
Drain-Source On-State Resistance	R _{DS(on)}	V _{GS} =-10V, I _D =-4A	-	67	85	mΩ
		V _{GS} =-4.5V, I _D =-2A	-	88	115	
Zero Gate Voltage Drain Current	I _{DSS}	V _{DS} =-60V, V _{GS} =0V	-	-	-1	uA
Gate-Source Leakage Current	I _{GSS}	V _{GS} =±20V, V _{DS} =0V	-	-	±100	nA
Dynamic (Note 6)						
Total Gate Charge	Q _g	V _{DS} =-30V, I _D =-4A, V _{GS} =-10V	-	17	23	nC
Gate-Source Charge	Q _{gs}		-	2.8	-	
Gate-Drain Charge	Q _{gd}		-	2.6	-	
Input Capacitance	C _{iss}	V _{DS} =-30V, V _{GS} =0V, f=1MHz	-	844	1200	pF
Output Capacitance	C _{oss}		-	52	95	
Reverse Transfer Capacitance	C _{rss}		-	35	65	
Gate resistance	R _g	f=1MHz	-	14	-	Ω
Turn-On Delay Time	t _{d(on)}	V _{DS} =-30V, I _D =-4A, V _{GS} =-10V, R _G =3Ω (Note 2)	-	4.9	-	ns
Turn-On Rise Time	t _r		-	3.1	-	
Turn-Off Delay Time	t _{d(off)}		-	27	-	
Turn-Off Fall Time	t _f		-	12	-	
Drain-Source Diode						
Diode Forward Current	I _S	T _C =25°C	-	-	-14	A
Pulsed Diode Forward Current	I _{SM}	(Package Limit)	-	-	-24	
Diode Forward Voltage	V _{SD}	I _S =-4A, V _{GS} =0V	-	-0.85	-1.3	V
Reverse Recovery Time	T _{rr}	V _{DD} =-30V, V _{GS} =0V, I _S =4A, dI _S /dt=100A/us	-	11	-	ns
Reverse Recovery Charge	Q _{rr}		-	6	-	nC

NOTES :

1. Pulse width ≤ 300us, Duty cycle ≤ 2%.
2. Essentially independent of operating temperature typical characteristics.
3. Chip capability with an R_{θJC}=4.1°C/W.
4. R_{θJA} is the sum of the junction-to-case and case-to-ambient thermal resistance where the case thermal reference is defined as the solder mounting surface of the drain pins. Mounted on a 1 inch² with 2oz.square pad of copper.
5. Repetitive rating, pulse width limited by junction temperature T_{J(MAX)}=175°C. Ratings are based on low frequency and duty cycles to keep initial T_J=25°C.
6. Guaranteed by design, not subject to production testing.

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TYPICAL CHARACTERISTIC CURVES

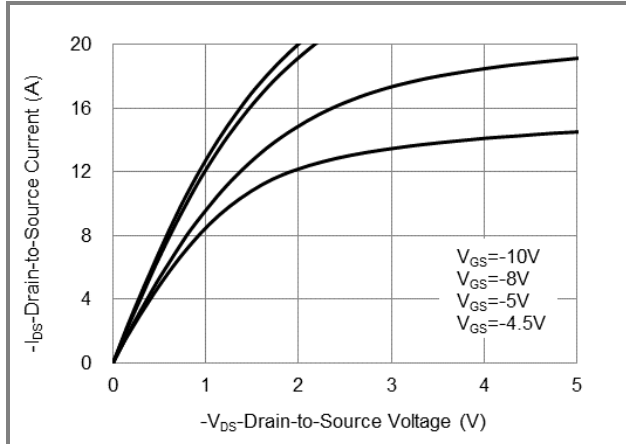


Fig.1 On-Region Characteristics

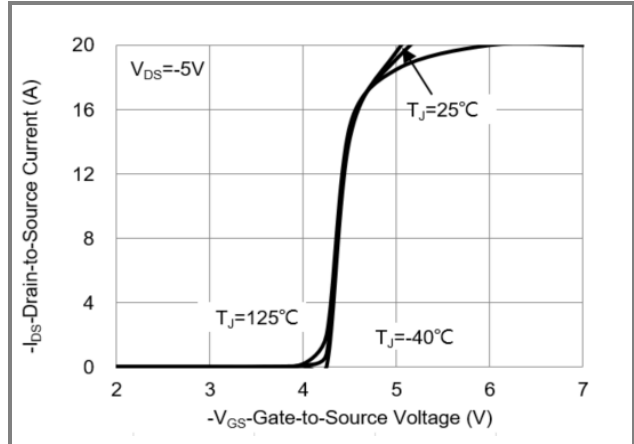


Fig.2 Transfer Characteristics

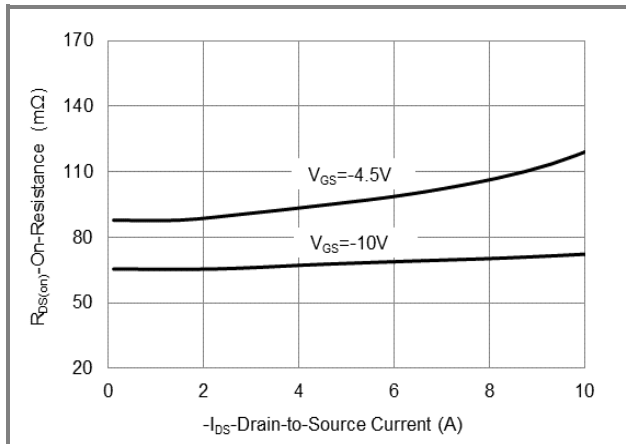


Fig.3 On-Resistance vs. Drain Current

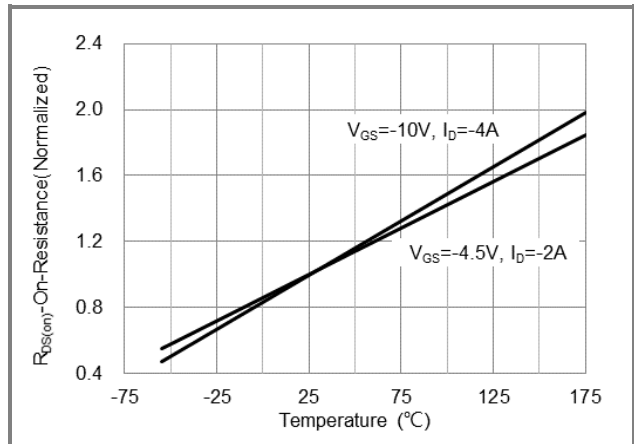


Fig.4 On-Resistance vs. Junction temperature

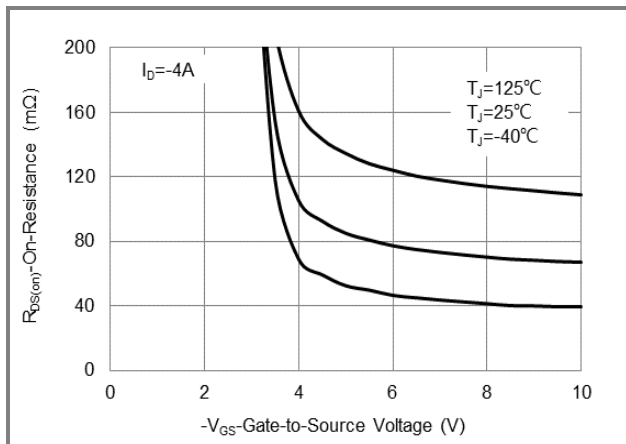


Fig.5 On-Resistance Variation with V_{GS}

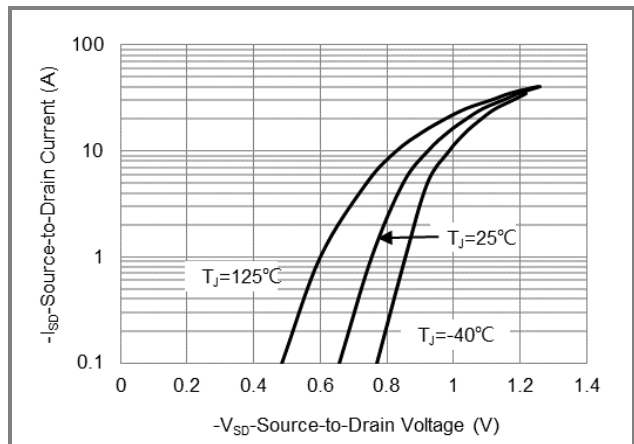


Fig.6 Source-Drain Diode Forward Voltage

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TYPICAL CHARACTERISTIC CURVES

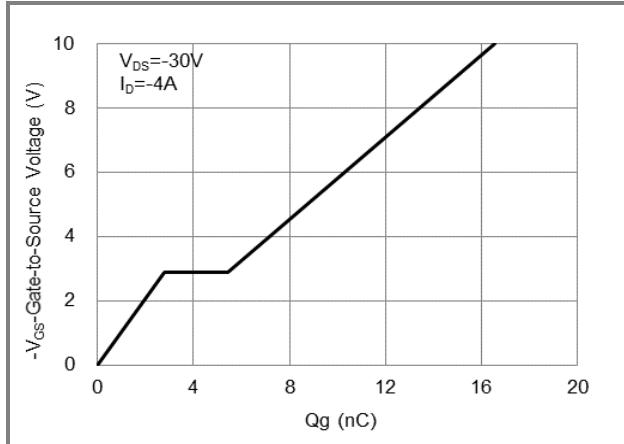


Fig.7 Gate-Charge Characteristics

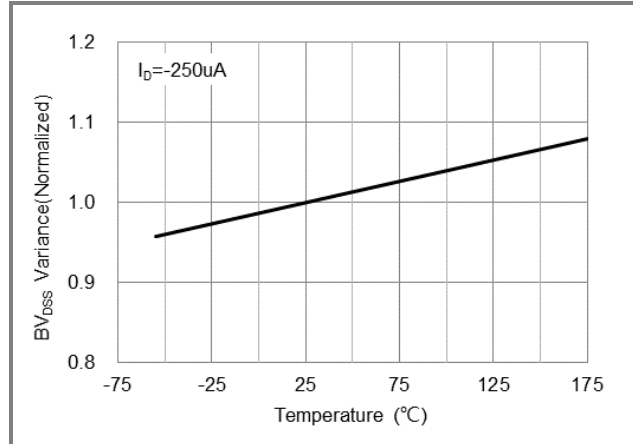


Fig.8 Breakdown Voltage Variation vs. Temperature

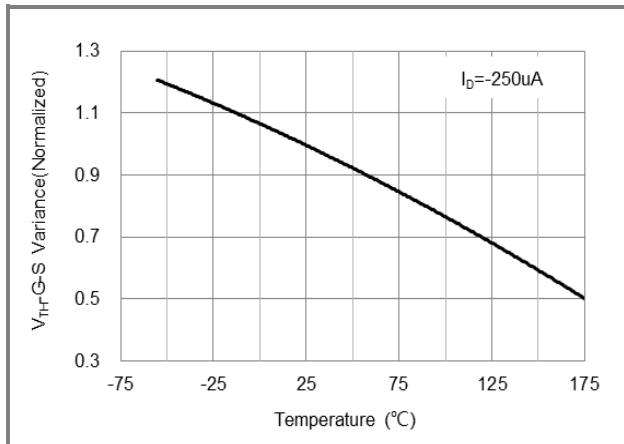


Fig.9 Threshold Voltage Variation with Temperature

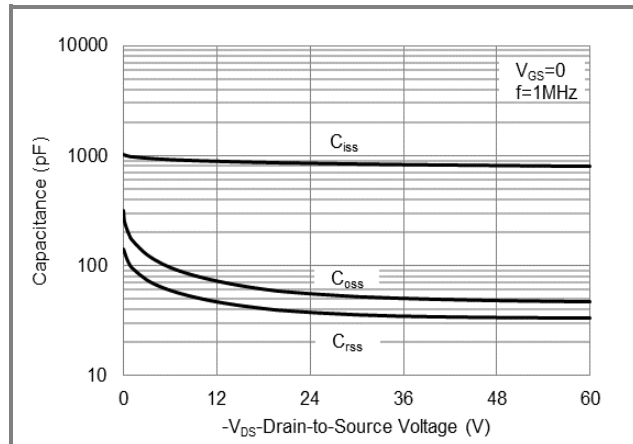


Fig.10 Capacitance vs. Drain-Source Voltage

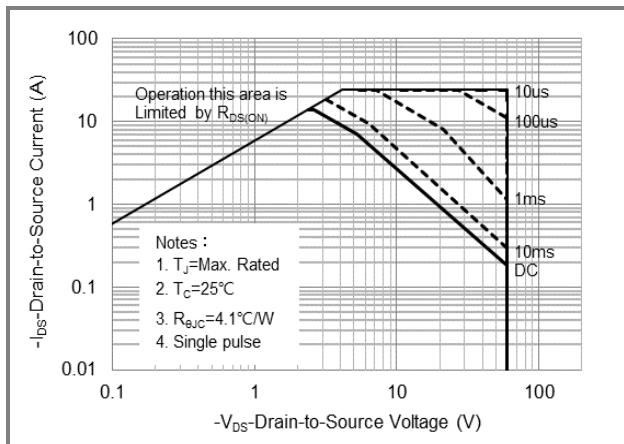


Fig.11 Maximum Safe Operating Area

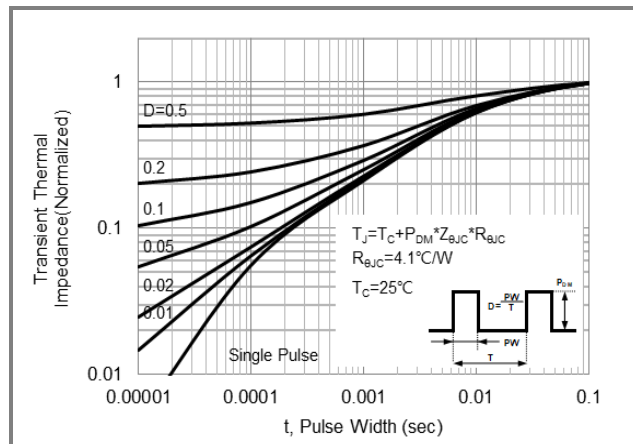


Fig.12 Normalized Transient Thermal Impedance

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