

PJQ54304UC-AU

30V N-Channel Enhancement Mode MOSFET

Voltage	30 V	Current	440 A
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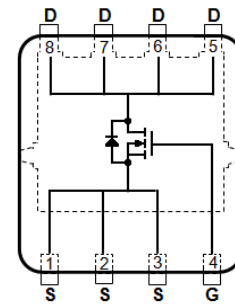
Features

- $R_{DS(ON)}$, $V_{GS}@10V$, $I_D@50A < 0.73m\Omega$
- $R_{DS(ON)}$, $V_{GS}@4.5V$, $I_D@50A < 1.2m\Omega$
- Logic Level Drive
- AEC-Q101 qualified
- Lead free in compliance with EU RoHS 2.0
- Green molding compound as per IEC 61249 standard

Mechanical Data

- Case : DFN5060XC-8L Package
- Terminals : Solderable per MIL-STD-750, Method 2026
- Approx. Weight : 0.098 grams

DFN5060XC-8L



Maximum Ratings and Thermal Characteristics ($T_A=25^\circ\text{C}$ unless otherwise noted)

PARAMETER		SYMBOL	LIMIT	UNIT
Drain-Source Voltage		V_{DS}	30	V
Gate-Source Voltage		V_{GS}	± 20	
Continuous Drain Current ^(Note 3)	$T_C=25^\circ\text{C}$	I_D	440	A
	$T_C=100^\circ\text{C}$		310	
Pulsed Drain Current ^(Note 1)	$T_C=25^\circ\text{C}$	I_{DM}	1200	
Power Dissipation	$T_C=25^\circ\text{C}$	P_D	268	W
	$T_C=100^\circ\text{C}$		134	
Continuous Drain Current ^(Note 4)	$T_A=25^\circ\text{C}$	I_D	52	A
	$T_A=70^\circ\text{C}$		43	
Power Dissipation	$T_A=25^\circ\text{C}$	P_D	3.8	W
	$T_A=70^\circ\text{C}$		2.6	
Single Pulse Avalanche Current ^(Note 6)		I_{AS}	33	A
Single Pulse Avalanche Energy ^(Note 6)		E_{AS}	545	mJ
Operating Junction and Storage Temperature Range		T_J, T_{STG}	-55~175	$^\circ\text{C}$
Thermal Resistance	Junction to Case	$R_{\theta JC}$	0.56	$^\circ\text{C/W}$
	Junction to Ambient	$R_{\theta JA}$ ^(Note 4)	40	
		$R_{\theta JA}$ ^(Note 5)	26 (Typ.)	

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Electrical Characteristics (T_A=25°C unless otherwise noted)

PARAMETER	SYMBOL	TEST CONDITION	MIN.	TYP.	MAX.	UNIT
Static						
Drain-Source Breakdown Voltage	BV _{DSS}	V _{GS} =0V, I _D =250uA	30	-	-	V
Gate Threshold Voltage	V _{GS(th)}	V _{DS} =V _{GS} , I _D =250uA	1.1	-	2.2	
Drain-Source On-State Resistance	R _{DS(on)}	V _{GS} =10V, I _D =50A	-	0.58	0.73	mΩ
		V _{GS} =4.5V, I _D =50A	-	0.9	1.2	
Zero Gate Voltage Drain Current	I _{DSS}	V _{DS} =30V, V _{GS} =0V	-	-	1	uA
Gate-Source Leakage Current	I _{GSS}	V _{GS} =±20V, V _{DS} =0V	-	-	±100	nA
Dynamic (Note 7)						
Total Gate Charge	Q _g	V _{DS} =24V, I _D =50A, V _{GS} =10V	-	262	350	nC
Gate-Source Charge	Q _{gs}		-	25	-	
Gate-Drain Charge	Q _{gd}		-	53	-	
Input Capacitance	C _{iss}	V _{DS} =25V, V _{GS} =0V, f=1MHz	-	13442	18000	pF
Output Capacitance	C _{oss}		-	1193	1600	
Reverse Transfer Capacitance	C _{rss}		-	1063	1400	
Gate resistance	R _g	f=1MHz	-	1.5	-	Ω
Turn-On Delay Time	t _{d(on)}	V _{DS} =24V, I _D =50A, V _{GS} =10V, R _G =3Ω (Note 2)	-	21	-	ns
Turn-On Rise Time	t _r		-	42	-	
Turn-Off Delay Time	t _{d(off)}		-	204	-	
Turn-Off Fall Time	t _f		-	111	-	
Drain-Source Diode						
Diode Forward Current	I _S	T _C =25°C	-	-	283	A
Pulsed Diode Forward Current	I _{SM}	(Package Limit)	-	-	1200	
Diode Forward Voltage	V _{SD}	I _S =90A, V _{GS} =0V	-	0.8	1.3	V
Reverse Recovery Time	T _{rr}	V _{DD} =24V, V _{GS} =0V,	-	26	-	ns
Reverse Recovery Charge	Q _{rr}	I _S =20A, dI _S /dt=100A/us	-	18	-	nC

NOTES :

1. Pulse width ≤ 100us, Duty cycle ≤ 2%.
2. Essentially independent of operating temperature typical characteristics.
3. Chip capability with an R_{θJC}=0.56°C/W.
4. R_{θJA} is the sum of the junction-to-case and case-to-ambient thermal resistance where the case thermal reference is defined as the solder mounting surface of the drain pins. Mounted on a 1 inch² with 2oz. square pad of copper.
5. Device on 2s2p FR4 PCB defined in accordance with JEDEC standards (JESD51-5,-7) PCB is vertical in still air.
6. E_{AS} is calculated based on the condition of L=1mH, I_{AS}=33A, V_{DD}=50V, V_{GS}=10V. 100% test at L=0.5mH, I_{AS}=35A in production.
7. Guaranteed by design, not subject to production testing.

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TYPICAL CHARACTERISTIC CURVES

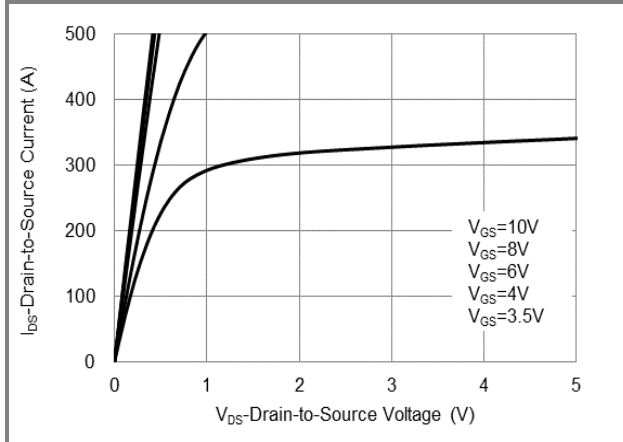


Fig.1 On-Region Characteristics

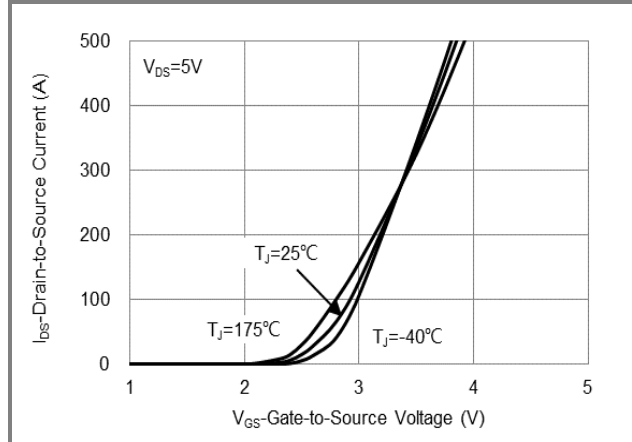


Fig.2 Transfer Characteristics

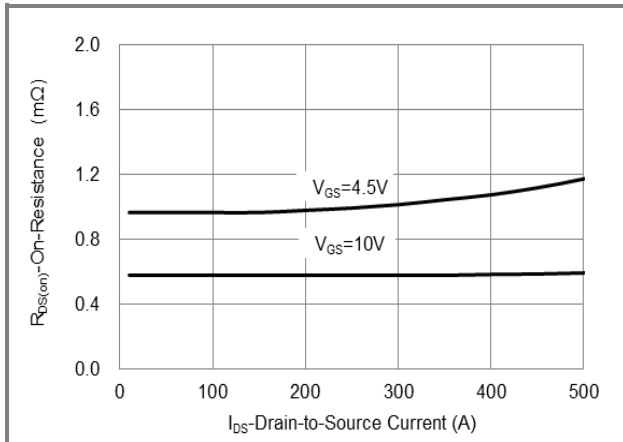


Fig.3 On-Resistance vs. Drain Current

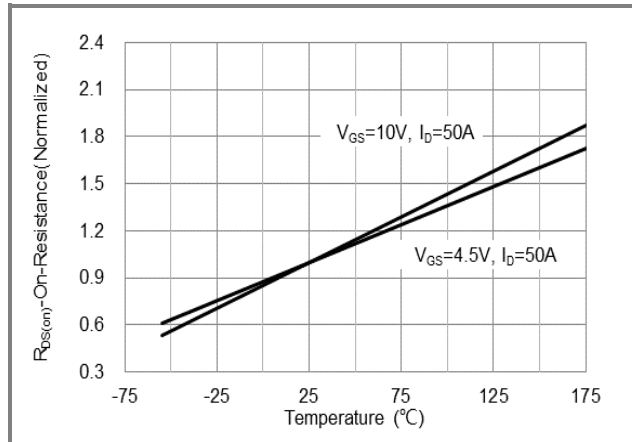


Fig.4 On-Resistance vs. Junction temperature

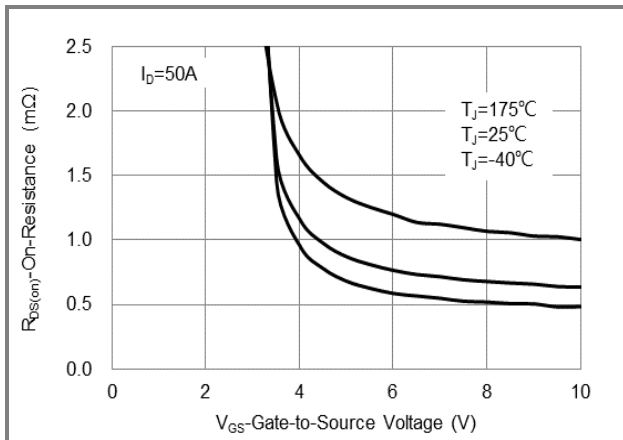


Fig.5 On-Resistance Variation with V_{GS}

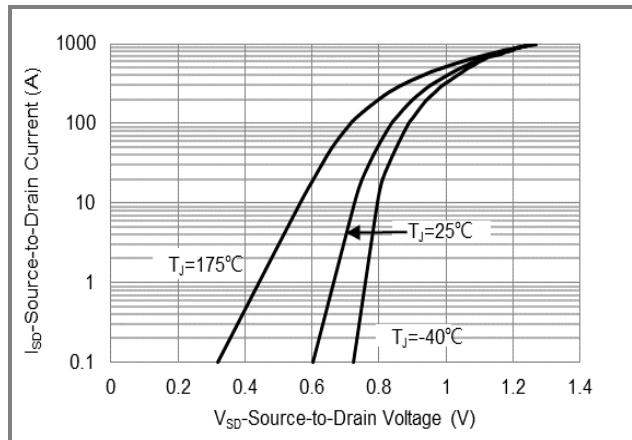
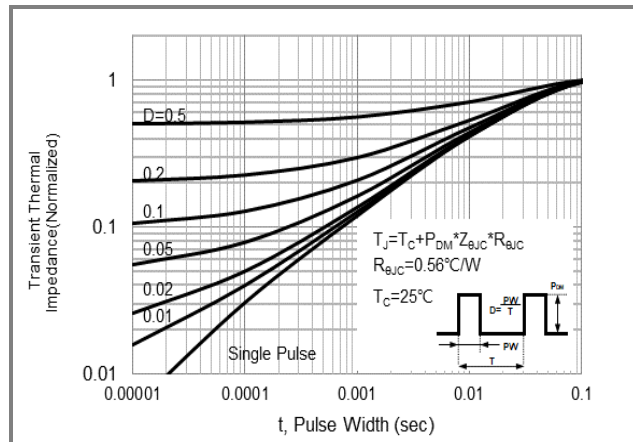
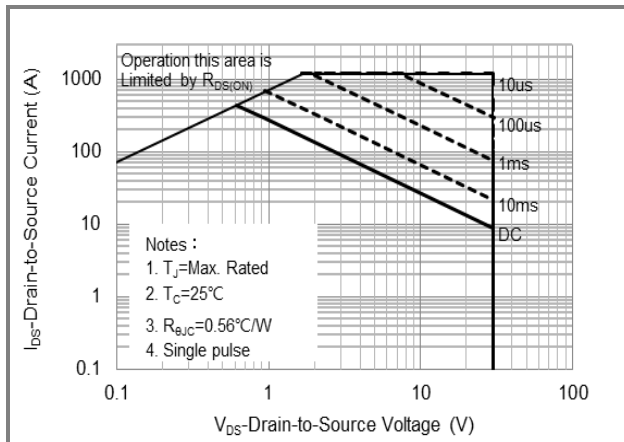
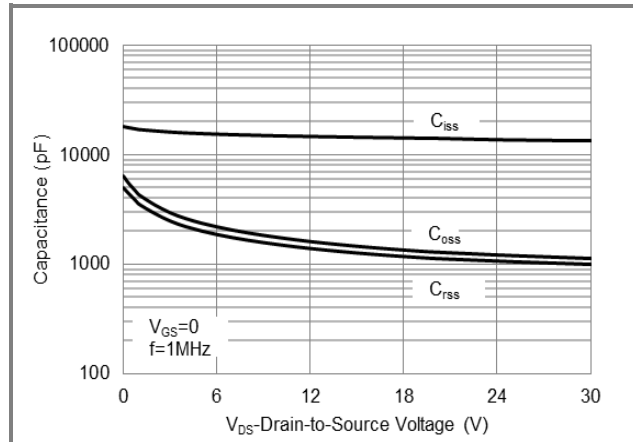
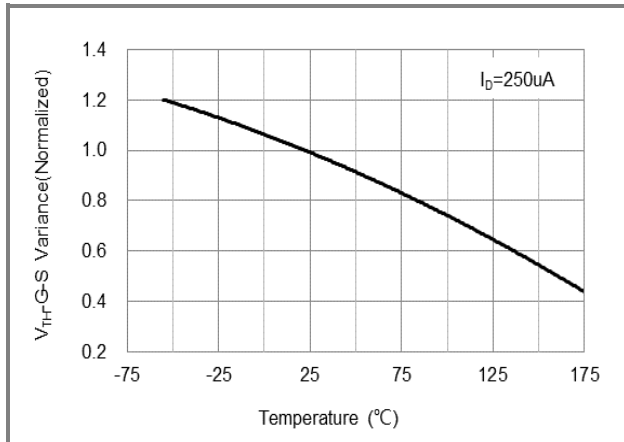
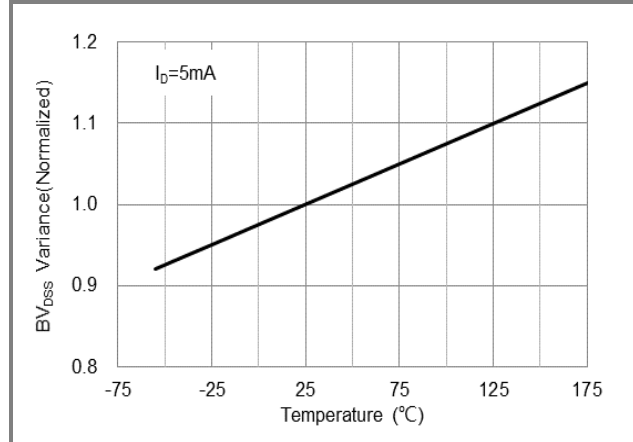
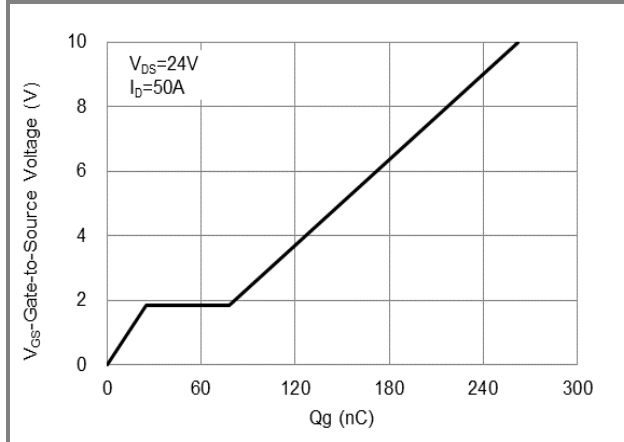


Fig.6 Source-Drain Diode Forward Voltage

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TYPICAL CHARACTERISTIC CURVES

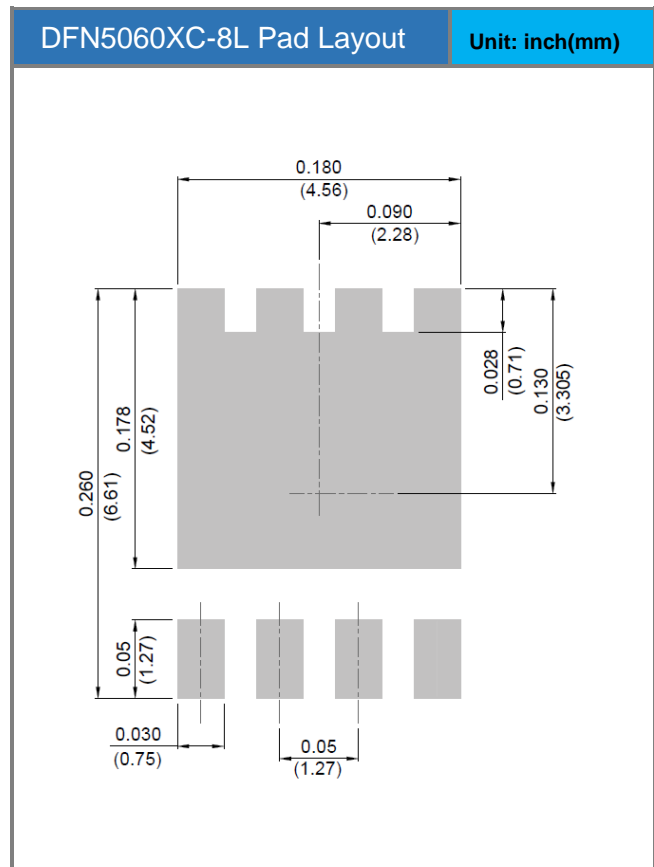
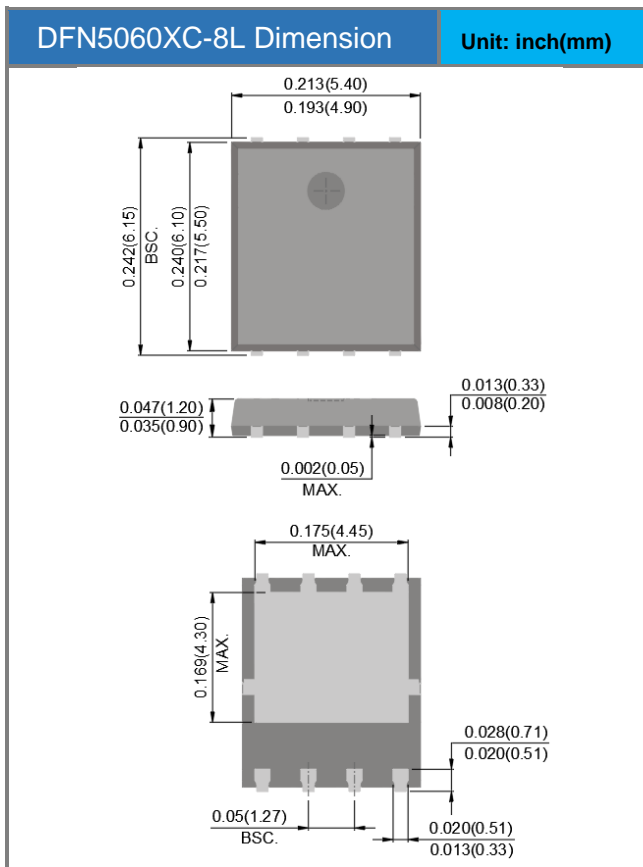


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Product and Packing Information

Part No.	Package Type	Packing Type	Marking
PJQ54304UC-AU	DFN5060XC-8L	3K pcs / 13" reel	54304UC

Packaging Information & Mounting Pad Layout



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