

PJQ54404VUC-AU

40V N-Channel Enhancement Mode MOSFET

Voltage	40 V	Current	240 A
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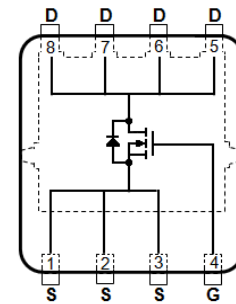
Features

- $R_{DS(ON)}$, $V_{GS}@10V$, $I_D@90A < 1.4m\Omega$
- $R_{DS(ON)}$, $V_{GS}@7V$, $I_D@50A < 1.8m\Omega$
- Standard Level Drive
- AEC-Q101 qualified
- Lead free in compliance with EU RoHS 2.0
- Green molding compound as per IEC 61249 standard

Mechanical Data

- Case : DFN5060XC-8L Package
- Terminals : Solderable per MIL-STD-750, Method 2026
- Approx. Weight : 0.098 grams

DFN5060XC-8L



Maximum Ratings and Thermal Characteristics ($T_A=25^\circ C$ unless otherwise noted)

PARAMETER		SYMBOL	LIMIT	UNIT
Drain-Source Voltage		V_{DS}	40	V
Gate-Source Voltage		V_{GS}	± 20	
Continuous Drain Current ^(Note 3)	$T_C=25^\circ C$	I_D	240	A
	$T_C=100^\circ C$		170	
Pulsed Drain Current ^(Note 1)	$T_C=25^\circ C$	I_{DM}	950	
Power Dissipation	$T_C=25^\circ C$	P_D	176	W
	$T_C=100^\circ C$		88	
Continuous Drain Current ^(Note 4)	$T_A=25^\circ C$	I_D	36	A
	$T_A=70^\circ C$		30	
Power Dissipation	$T_A=25^\circ C$	P_D	3.8	W
	$T_A=70^\circ C$		2.6	
Single Pulse Avalanche Current ^(Note 6)		I_{AS}	33	A
Single Pulse Avalanche Energy ^(Note 6)		E_{AS}	545	mJ
Operating Junction and Storage Temperature Range		T_J, T_{STG}	-55~175	$^\circ C$
Thermal Resistance	Junction to Case	$R_{\theta JC}$	0.85	$^\circ C/W$
	Junction to Ambient	$R_{\theta JA}$ ^(Note 4)	40	
		$R_{\theta JA}$ ^(Note 5)	26 (Typ.)	

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Electrical Characteristics (T_A=25°C unless otherwise noted)

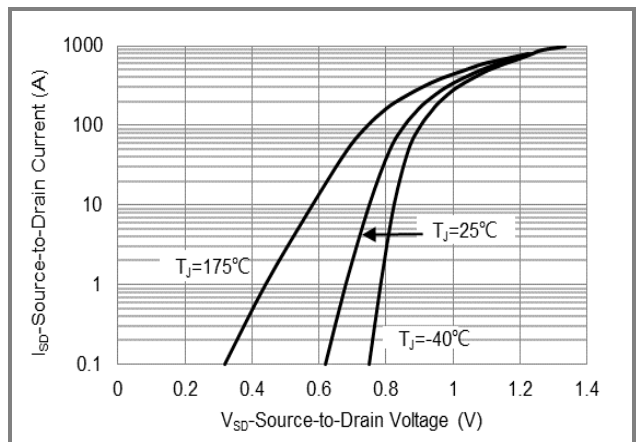
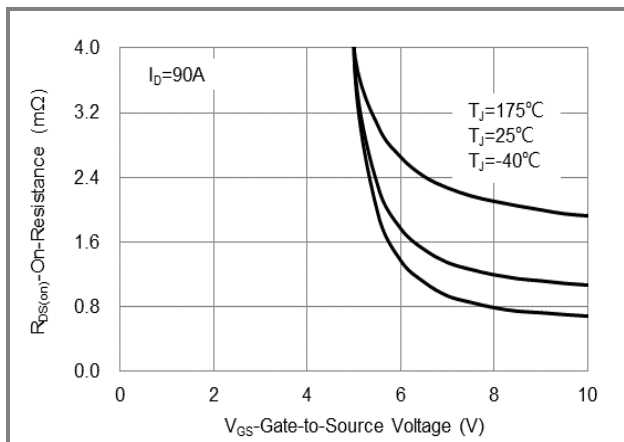
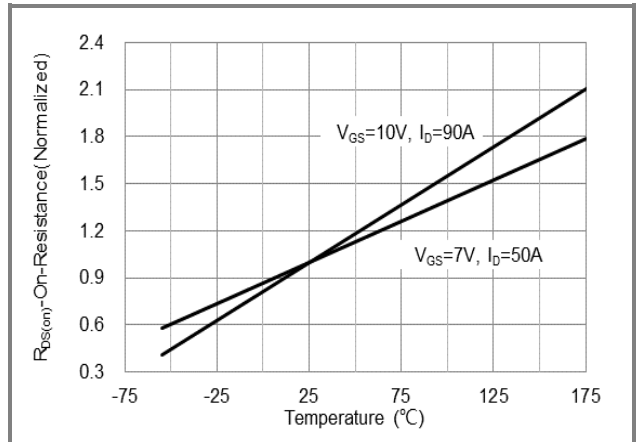
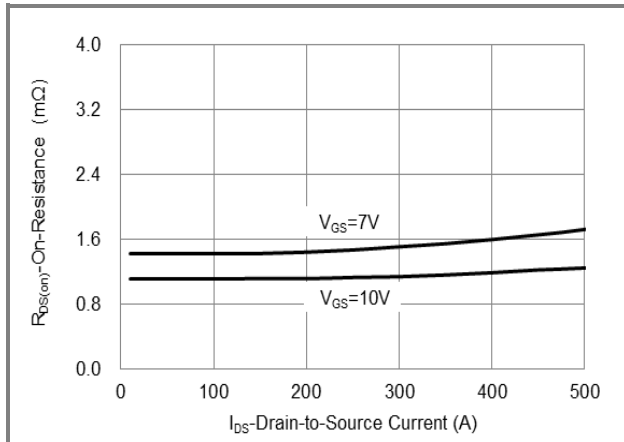
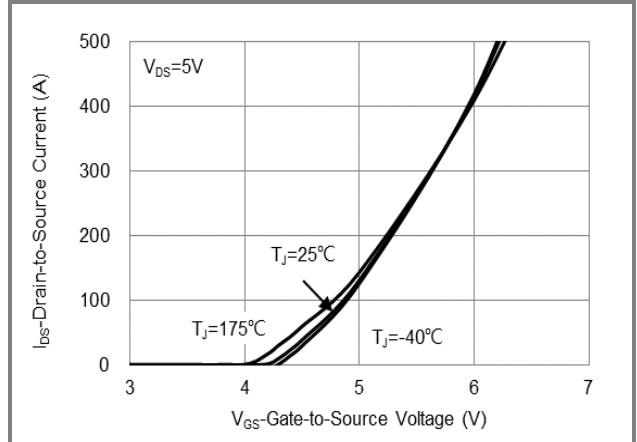
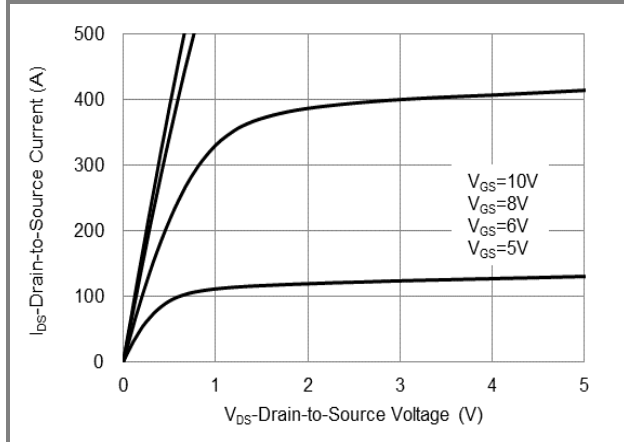
PARAMETER	SYMBOL	TEST CONDITION	MIN.	TYP.	MAX.	UNIT
Static						
Drain-Source Breakdown Voltage	BV _{DSS}	V _{GS} =0V, I _D =250uA	40	-	-	V
Gate Threshold Voltage	V _{GS(th)}	V _{DS} =V _{GS} , I _D =250uA	2	2.8	3.5	
Drain-Source On-State Resistance	R _{DS(on)}	V _{GS} =10V, I _D =90A	-	1.1	1.4	mΩ
		V _{GS} =7V, I _D =50A	-	1.41	1.8	
Zero Gate Voltage Drain Current	I _{DSS}	V _{DS} =40V, V _{GS} =0V	-	-	1	uA
Gate-Source Leakage Current	I _{GSS}	V _{GS} =±20V, V _{DS} =0V	-	-	±100	nA
Dynamic ^(Note 7)						
Total Gate Charge	Q _g	V _{DS} =32V, I _D =50A, V _{GS} =10V	-	206	270	nC
Gate-Source Charge	Q _{gs}		-	48	-	
Gate-Drain Charge	Q _{gd}		-	50	-	
Input Capacitance	C _{iss}	V _{DS} =25V, V _{GS} =0V, f=1MHz	-	13310	17500	pF
Output Capacitance	C _{oss}		-	831	1170	
Reverse Transfer Capacitance	C _{rss}		-	656	920	
Gate resistance	R _g	f=1MHz	-	1.7	-	Ω
Turn-On Delay Time	td _(on)	V _{DS} =32V, I _D =50A, V _{GS} =10V, R _G =3Ω (Note 2)	-	37	-	ns
Turn-On Rise Time	tr		-	47	-	
Turn-Off Delay Time	td _(off)		-	115	-	
Turn-Off Fall Time	tf		-	50	-	
Drain-Source Diode						
Diode Forward Current	I _S	T _C =25°C	-	-	135	A
Pulsed Diode Forward Current	I _{SM}	(Package Limit)	-	-	950	
Diode Forward Voltage	V _{SD}	I _S =90A, V _{GS} =0V	-	0.8	1.3	V
Reverse Recovery Time	T _{rr}	V _{DD} =32V, V _{GS} =0V,	-	29	-	ns
Reverse Recovery Charge	Q _{rr}	I _S =20A, di _S /dt=100A/us	-	23	-	nC

NOTES :

1. Pulse width ≤ 100us, Duty cycle ≤ 2%.
2. Essentially independent of operating temperature typical characteristics.
3. Chip capability with an R_{θJC}=0.85°C/W.
4. R_{θJA} is the sum of the junction-to-case and case-to-ambient thermal resistance where the case thermal reference is defined as the solder mounting surface of the drain pins. Mounted on a 1 inch² with 2oz. square pad of copper.
5. Device on 2s2p FR4 PCB defined in accordance with JEDEC standards (JESD51-5,-7) PCB is vertical in still air.
6. E_{AS} is calculated based on the condition of L=1mH, I_{AS}=33A, V_{DD}=30V, V_{GS}=10V. 100% test at L=0.5mH, I_{AS}=35A in production.
7. Guaranteed by design, not subject to production testing.

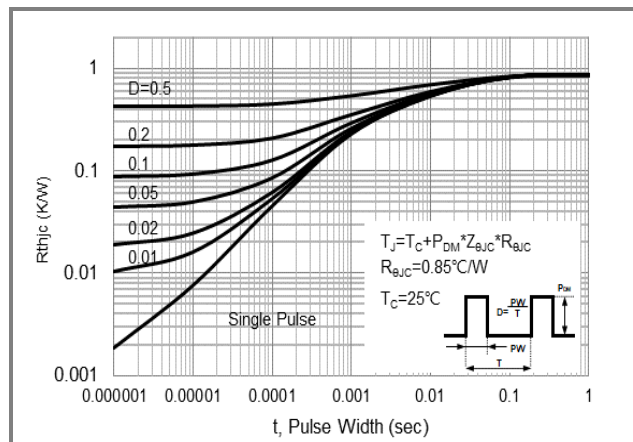
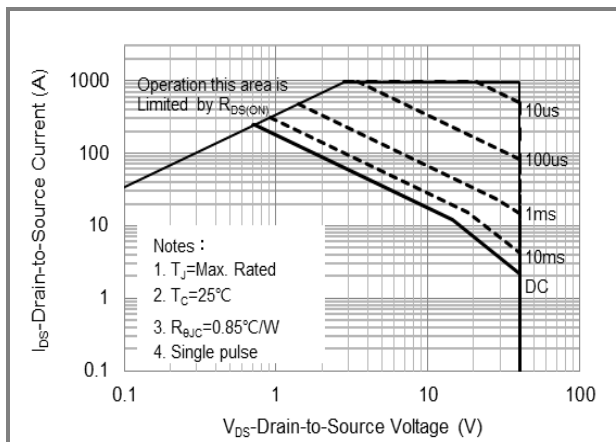
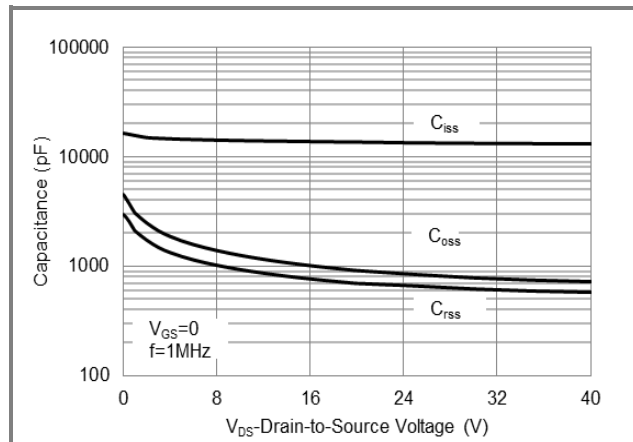
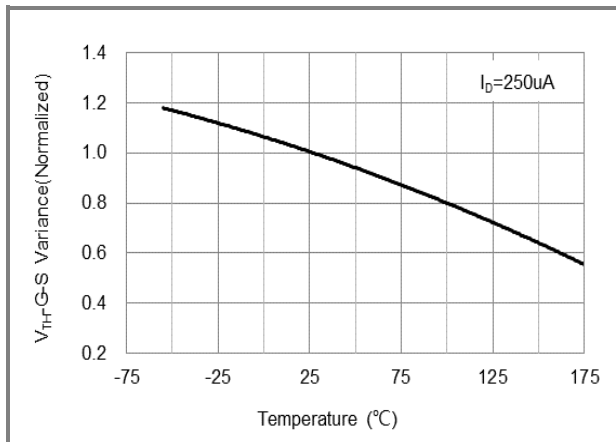
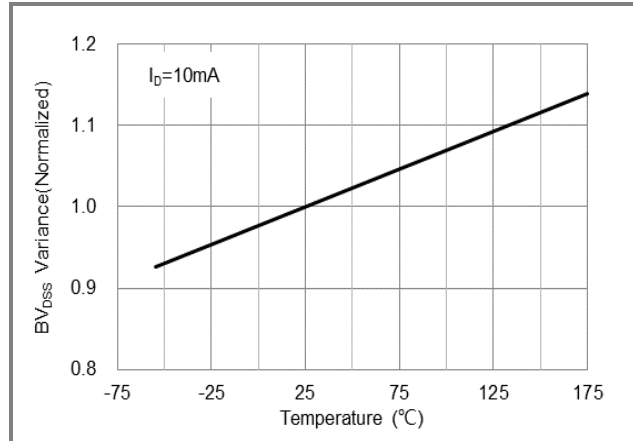
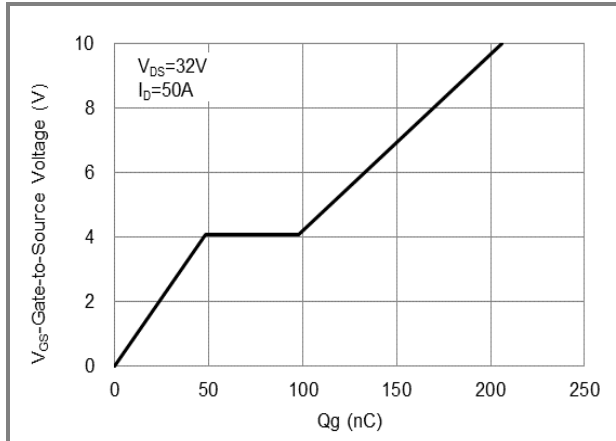
PJQ54404VUC-AU

TYPICAL CHARACTERISTIC CURVES



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TYPICAL CHARACTERISTIC CURVES

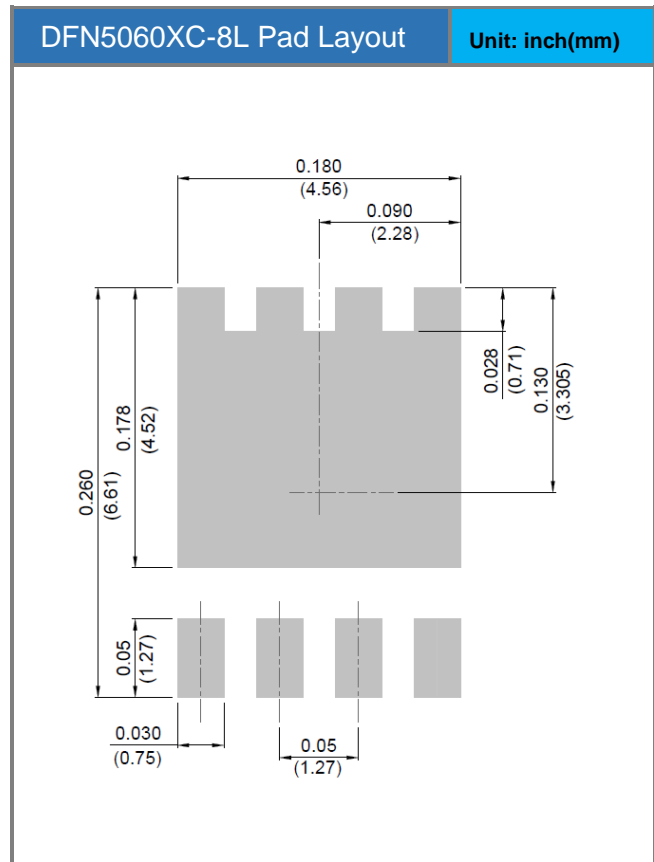
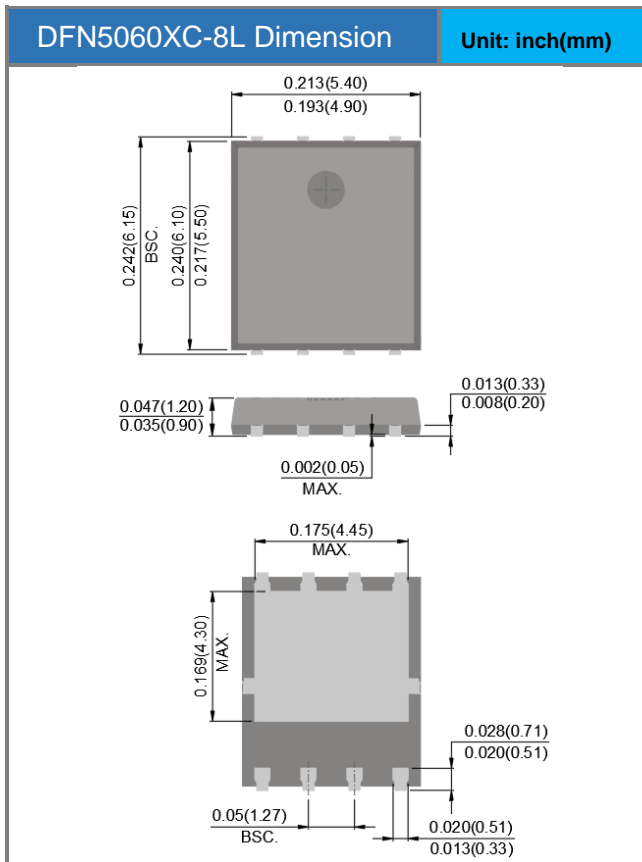


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Product and Packing Information

Part No.	Package Type	Packing Type	Marking
PJQ54404VUC-AU	DFN5060XC-8L	3K pcs / 13" reel	54404VUC

Packaging Information & Mounting Pad Layout



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