



PJQ5453E-AU

40V P-Channel Enhancement Mode MOSFET

Voltage -40 V **Current** -61 A

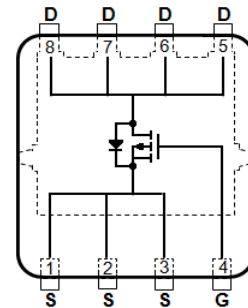
Features

- $R_{DS(ON)}$, $V_{GS}@-10V$, $I_D@-20A < 11.3m\Omega$
- $R_{DS(ON)}$, $V_{GS}@-4.5V$, $I_D@-10A < 17.2m\Omega$
- 100% UIS tested
- Reliable and Rugged
- AEC-Q101 qualified
- Lead free in compliance with EU RoHS 2.0
- Green molding compound as per IEC 61249 standard

Mechanical Data

- Case : DFN5060-8L Package
- Terminals : Solderable per MIL-STD-750, Method 2026
- Approx. Weight : 0.08 grams

DFN5060-8L



Maximum Ratings and Thermal Characteristics ($T_A=25^\circ C$ unless otherwise noted)

PARAMETER		SYMBOL	LIMIT	UNITS
Drain-Source Voltage		V_{DS}	-40	V
Gate-Source Voltage		V_{GS}	± 25	
Continuous Drain Current ^(Note 3)	$T_C=25^\circ C$	I_D	-61	A
	$T_C=100^\circ C$		-43	
Pulsed Drain Current ^(Note 1)	$T_C=25^\circ C$	I_{DM}	-171	
Power Dissipation	$T_C=25^\circ C$	P_D	75	W
	$T_C=100^\circ C$		38	
Continuous Drain Current ^(Note 4)	$T_A=25^\circ C$	I_D	-12.8	A
	$T_A=70^\circ C$		-10.7	
Power Dissipation	$T_A=25^\circ C$	P_D	3.3	W
	$T_A=70^\circ C$		2.2	
Single Pulse Avalanche Energy ^(Note 5)		E_{AS}	121	mJ
Operating Junction and Storage Temperature Range		T_J, T_{STG}	-55~175	$^\circ C$
Thermal Resistance ^(Note 4)	Junction to Case	$R_{\theta JC}$	2	$^\circ C/W$
	Junction to Ambient	$R_{\theta JA}$	45	



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Electrical Characteristics ($T_A=25^\circ\text{C}$ unless otherwise noted)

PARAMETER	SYMBOL	TEST CONDITION	MIN.	TYP.	MAX.	UNITS
Static						
Drain-Source Breakdown Voltage	BV_{DSS}	$V_{GS}=0V, I_D=-250\mu A$	-40	-	-	V
Gate Threshold Voltage	$V_{GS(th)}$	$V_{DS}=V_{GS}, I_D=-250\mu A$	-1	-1.7	-2.5	
Drain-Source On-State Resistance	$R_{DS(on)}$	$V_{GS}=-10V, I_D=-20A$	-	9	11.3	m Ω
		$V_{GS}=-4.5V, I_D=-10A$	-	13.2	17.2	
Zero Gate Voltage Drain Current	I_{DSS}	$V_{DS}=-40V, V_{GS}=0V$	-	-	-1	μA
Gate-Source Leakage Current	I_{GSS}	$V_{GS}=\pm 25V, V_{DS}=0V$	-	-	± 100	nA
Dynamic (Note 6)						
Total Gate Charge	Q_g	$V_{DS}=-32V, I_D=-20A,$ $V_{GS}=-10V$	-	56	-	nC
Gate-Source Charge	Q_{gs}		-	8.4	-	
Gate-Drain Charge	Q_{gd}		-	18	-	
Input Capacitance	C_{iss}	$V_{DS}=-25V, V_{GS}=0V,$ $f=1MHz$	-	2858	-	pF
Output Capacitance	C_{oss}		-	228	-	
Reverse Transfer Capacitance	C_{rss}		-	179	-	
Gate resistance	R_g	$f=1MHz$	-	2.9	-	Ω
Turn-On Delay Time	$t_{d(on)}$	$V_{DS}=-32, I_D=-20A,$ $V_{GS}=-10V, R_G=3\Omega$ (Note 2)	-	11	-	ns
Turn-On Rise Time	t_r		-	10	-	
Turn-Off Delay Time	$t_{d(off)}$		-	47	-	
Turn-Off Fall Time	t_f		-	24	-	
Drain-Source Diode						
Diode Forward Current	I_S	$T_C=25^\circ\text{C}$	-	-	-61	A
Pulsed Diode Forward Current	I_{SM}		-	-	-171	
Diode Forward Voltage	V_{SD}	$I_S=-20A, V_{GS}=0V$	-	-0.85	-1.3	V
Reverse Recovery Time	T_{rr}	$V_{GS}=0V, I_S=-20A$	-	29	-	ns
Reverse Recovery Charge	Q_{rr}	$dI_S/dt=100A/\mu s$	-	24	-	nC

NOTES :

1. Pulse width $\leq 300\mu s$, Duty cycle $\leq 2\%$.
2. Essentially independent of operating temperature typical characteristics.
3. The maximum current rating is package limited.
4. $R_{\theta JA}$ is the sum of the junction-to-case and case-to-ambient thermal resistance where the case thermal reference is defined as the solder mounting surface of the drain pins. Mounted on a 1 inch² with 2oz. square pad of copper.
5. The test condition is $L=0.5mH, I_{AS}=-22A, V_{DD}=-30V, V_{GS}=-10V$, Starting $T_J=25^\circ\text{C}$.
6. Guaranteed by design, not subject to production testing.



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TYPICAL CHARACTERISTIC CURVES

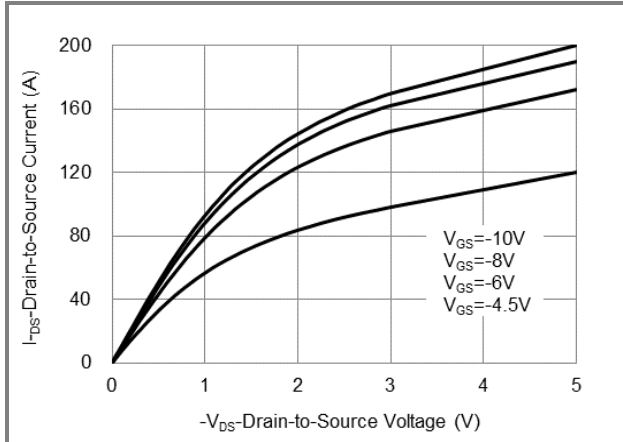


Fig.1 On-Region Characteristics

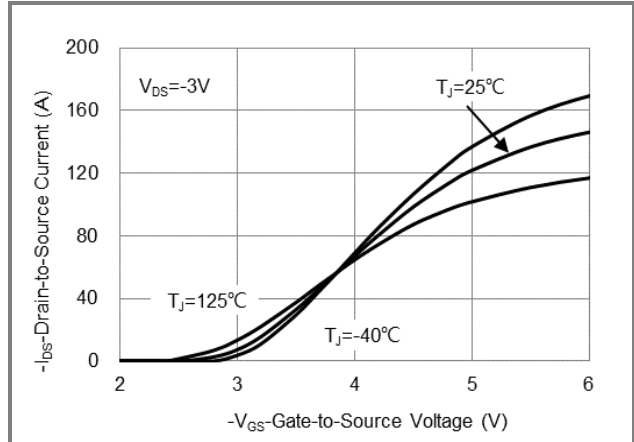


Fig.2 Transfer Characteristics

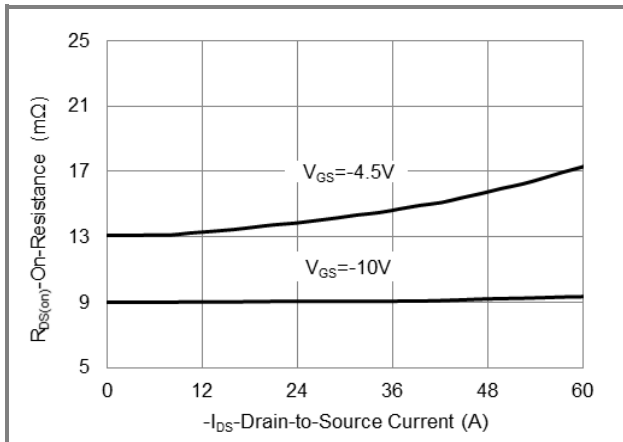


Fig.3 On-Resistance vs. Drain Current

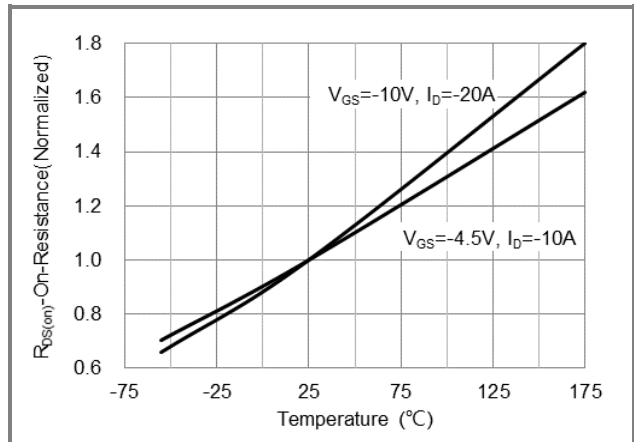


Fig.4 On-Resistance vs. Junction temperature

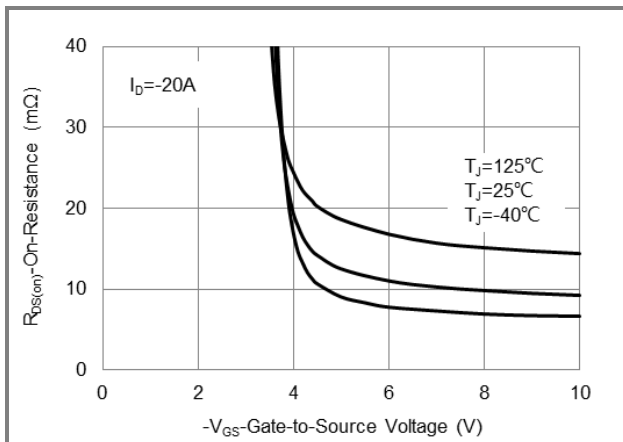


Fig.5 On-Resistance Variation with V_{GS}

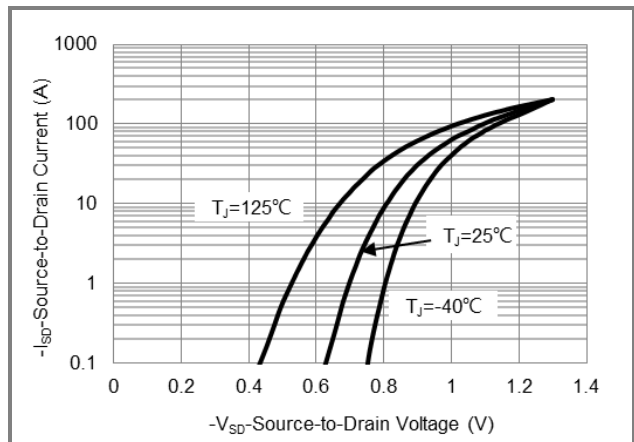


Fig.6 Source-Drain Diode Forward Voltage



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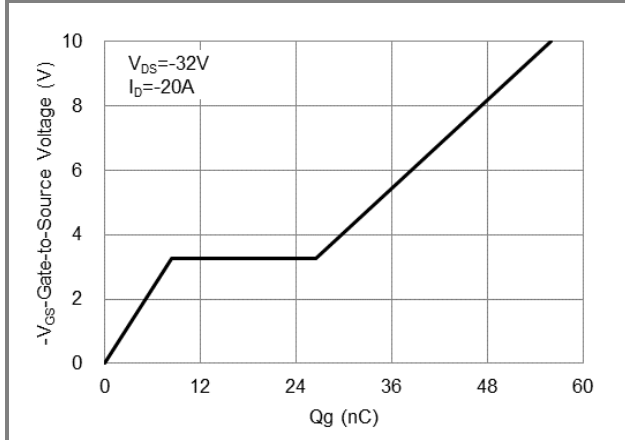


Fig.7 Gate-Charge Characteristics

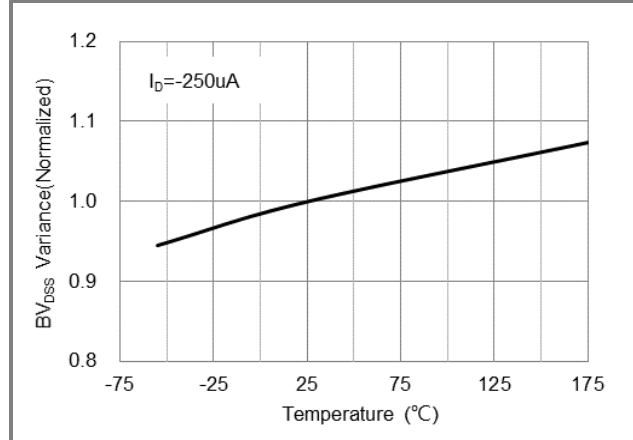


Fig.8 Breakdown Voltage Variation vs. Temperature

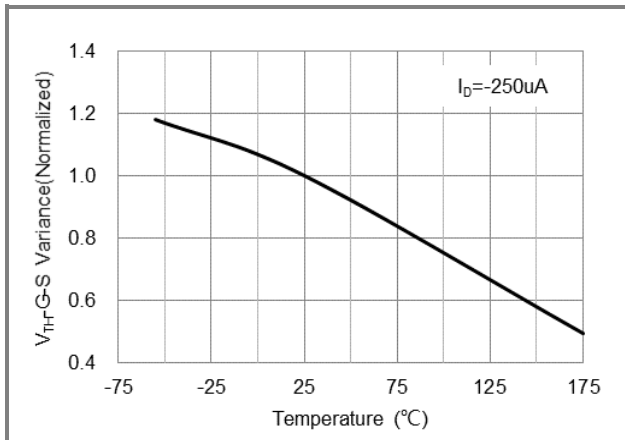


Fig.9 Threshold Voltage Variation with Temperature

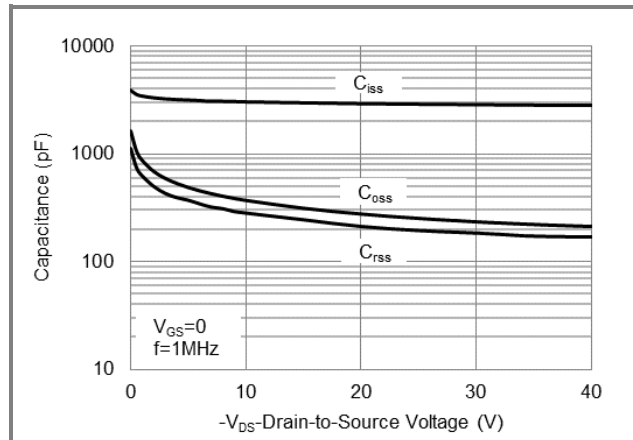


Fig.10 Capacitance vs. Drain-Source Voltage

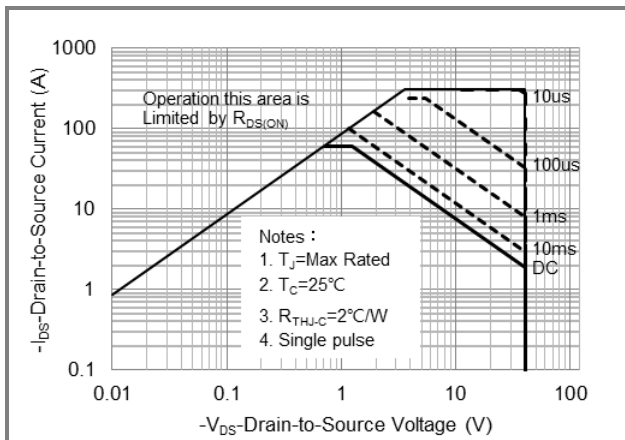


Fig.11 Maximum Safe Operating Area

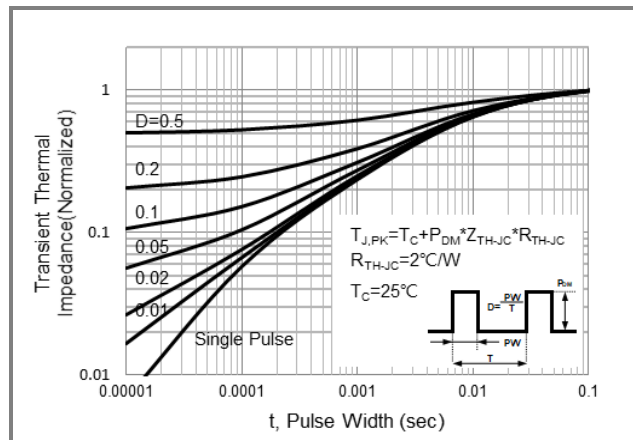


Fig.12 Normalized Transient Thermal Impedance

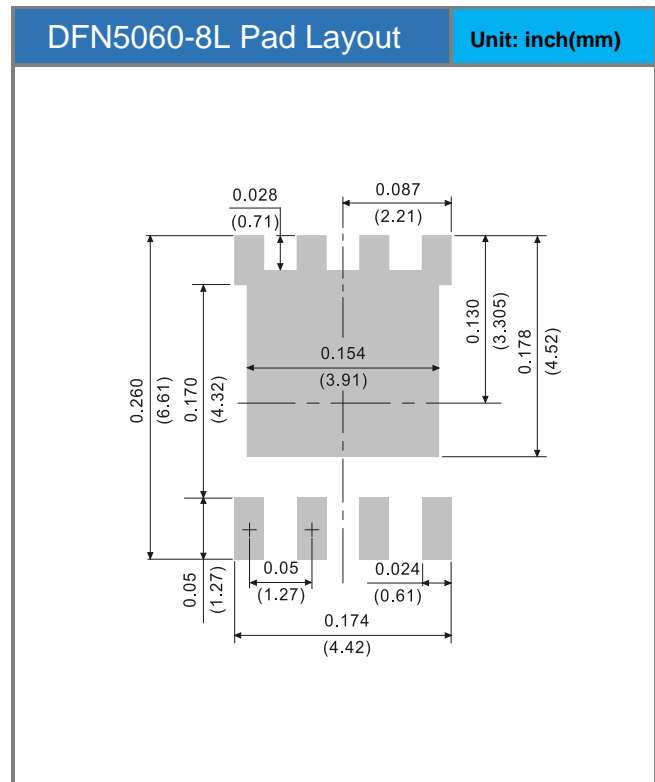
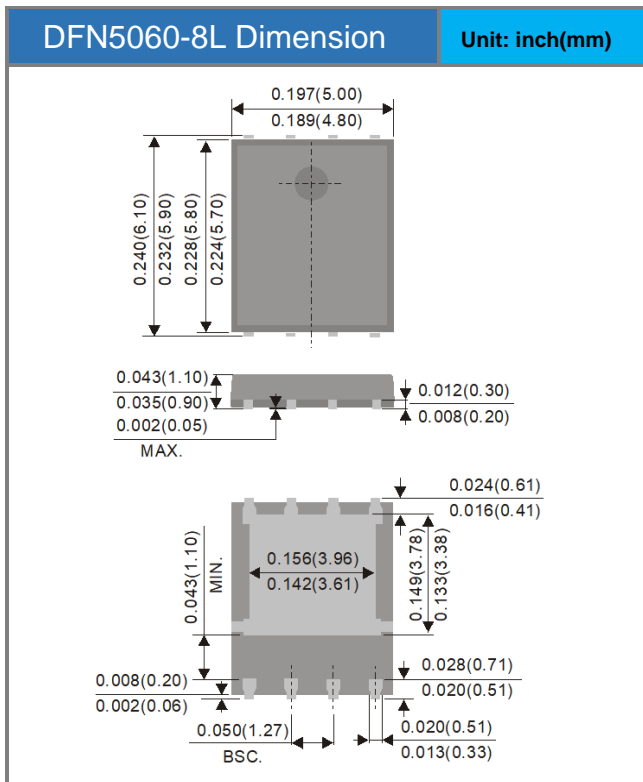


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Product and Packing Information

Part No.	Package Type	Packing Type	Marking
PJQ5453E-AU	DFN5060-8L	3K pcs / 13" reel	Q5453E

Packaging Information & Mounting Pad Layout





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