

# PJQ5534-AU

## 30V N-Channel Enhancement Mode MOSFET

<b>Voltage</b>	<b>30 V</b>	<b>Current</b>	<b>39 A</b>
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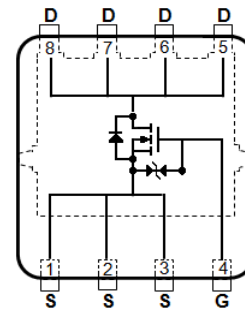
### Features

- $R_{DS(ON)}$ ,  $V_{GS}@10V$ ,  $I_D@20A < 9.3m\Omega$
- $R_{DS(ON)}$ ,  $V_{GS}@4.5V$ ,  $I_D@10A < 14.7m\Omega$
- Excellent FOM
- Logic Level Drive
- AEC-Q101 qualified
- Lead free in compliance with EU RoHS 2.0
- Green molding compound as per IEC 61249 standard

### Mechanical Data

- Case : DFN5060-8L Package
- Terminals : Solderable per MIL-STD-750, Method 2026
- Approx. Weight : 0.08 grams

DFN5060-8L



### Maximum Ratings and Thermal Characteristics ( $T_A=25^\circ\text{C}$ unless otherwise noted)

PARAMETER		SYMBOL	LIMIT	UNITS
Drain-Source Voltage		$V_{DS}$	30	V
Gate-Source Voltage		$V_{GS}$	$\pm 20$	
Continuous Drain Current <sup>(Note 3)</sup>	$T_C=25^\circ\text{C}$	$I_D$	39	A
	$T_C=100^\circ\text{C}$		28	
Pulsed Drain Current <sup>(Note 1)</sup>	$T_C=25^\circ\text{C}$	$I_{DM}$	156	
Power Dissipation	$T_C=25^\circ\text{C}$	$P_D$	23	W
	$T_C=100^\circ\text{C}$		11.5	
Continuous Drain Current <sup>(Note 4)</sup>	$T_A=25^\circ\text{C}$	$I_D$	15	A
	$T_A=70^\circ\text{C}$		12.5	
Power Dissipation	$T_A=25^\circ\text{C}$	$P_D$	3.3	W
	$T_A=70^\circ\text{C}$		2.3	
Single Pulse Avalanche Energy <sup>(Note 5)</sup>		$E_{AS}$	16	mJ
Operating Junction and Storage Temperature Range		$T_J, T_{STG}$	-55~175	$^\circ\text{C}$
Thermal Resistance <sup>(Note 4)</sup>	Junction to Case	$R_{\theta JC}$	6.5	$^\circ\text{C/W}$
	Junction to Ambient	$R_{\theta JA}$	45	

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## Electrical Characteristics (T<sub>A</sub>=25°C unless otherwise noted)

PARAMETER	SYMBOL	TEST CONDITION	MIN.	TYP.	MAX.	UNITS
<b>Static</b>						
Drain-Source Breakdown Voltage	BV <sub>DSS</sub>	V <sub>GS</sub> =0V, I <sub>D</sub> =250uA	30	-	-	V
Gate Threshold Voltage	V <sub>GS(th)</sub>	V <sub>DS</sub> =V <sub>GS</sub> , I <sub>D</sub> =250uA	1.3	1.8	2.5	
Drain-Source On-State Resistance	R <sub>DS(on)</sub>	V <sub>GS</sub> =10V, I <sub>D</sub> =20A	-	7.4	9.3	mΩ
		V <sub>GS</sub> =4.5V, I <sub>D</sub> =10A	-	11.3	14.7	
Zero Gate Voltage Drain Current	I <sub>DSS</sub>	V <sub>DS</sub> =30V, V <sub>GS</sub> =0V	-	-	±1	uA
Gate-Source Leakage Current	I <sub>GSS</sub>	V <sub>GS</sub> =±20V, V <sub>DS</sub> =0V	-	-	±10	uA
		V <sub>GS</sub> =±10V, V <sub>DS</sub> =0V	-	-	±1	
<b>Dynamic</b> (Note 6)						
Total Gate Charge	Q <sub>g</sub>	V <sub>DS</sub> =24V, I <sub>D</sub> =20A, V <sub>GS</sub> =10V	-	9.5	-	nC
Gate-Source Charge	Q <sub>gs</sub>		-	1.2	-	
Gate-Drain Charge	Q <sub>gd</sub>		-	1.8	-	
Input Capacitance	C <sub>iss</sub>	V <sub>DS</sub> =25V, V <sub>GS</sub> =0V, f=1MHz	-	490	-	pF
Output Capacitance	C <sub>oss</sub>		-	270	-	
Reverse Transfer Capacitance	C <sub>rss</sub>		-	23	-	
Gate resistance	R <sub>g</sub>	f=1MHz	-	2	-	Ω
Turn-On Delay Time	t <sub>d(on)</sub>	V <sub>DS</sub> =24V, I <sub>D</sub> =20A, V <sub>GS</sub> =10V, R <sub>G</sub> =3Ω (Note 2)	-	8.8	-	ns
Turn-On Rise Time	t <sub>r</sub>		-	7	-	
Turn-Off Delay Time	t <sub>d(off)</sub>		-	18	-	
Turn-Off Fall Time	t <sub>f</sub>		-	12	-	
<b>Drain-Source Diode</b>						
Diode Forward Current	I <sub>S</sub>	T <sub>C</sub> =25°C	-	-	39	A
Pulsed Diode Forward Current	I <sub>SM</sub>		-	-	156	
Diode Forward Voltage	V <sub>SD</sub>	I <sub>S</sub> =20A, V <sub>GS</sub> =0V	-	0.9	1.1	V
Reverse Recovery Time	T <sub>rr</sub>	V <sub>GS</sub> =0V, I <sub>S</sub> =20A	-	20	-	ns
Reverse Recovery Charge	Q <sub>rr</sub>	dI <sub>S</sub> /dt=100A/us	-	8.5	-	nC

**NOTES :**

1. Pulse width ≤ 100us, Duty cycle ≤ 2%.
2. Essentially independent of operating temperature typical characteristics.
3. Chip capability with an R<sub>θJC</sub>=6.5°C/W.
4. R<sub>θJA</sub> is the sum of the junction-to-case and case-to-ambient thermal resistance where the case thermal reference is defined as the solder mounting surface of the drain pins. Mounted on a 1 inch<sup>2</sup> with 2oz.square pad of copper.
5. The test condition is L=0.5mH, I<sub>AS</sub>=8A, V<sub>DD</sub>=30V, V<sub>GS</sub>=10V, Starting T<sub>J</sub>=25°C. the chip is about to carry I<sub>AS</sub>≈16A.
6. Guaranteed by design, not subject to production testing.

# PJQ5534-AU

## TYPICAL CHARACTERISTIC CURVES

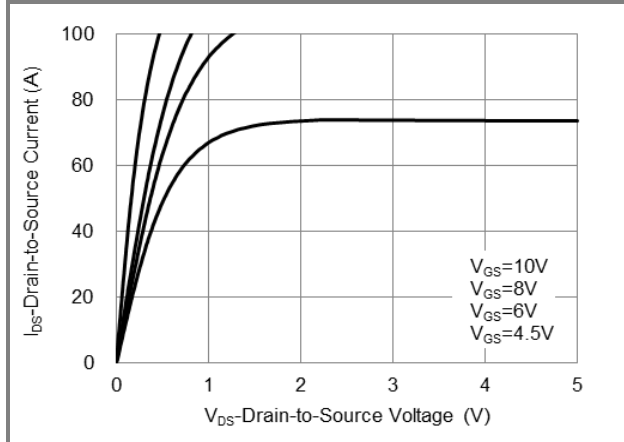


Fig.1 On-Region Characteristics

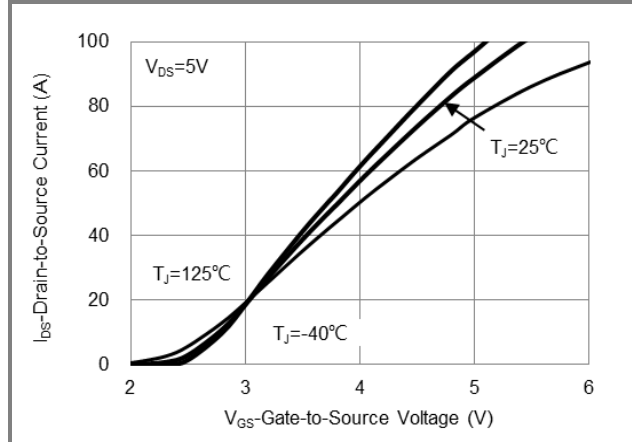


Fig.2 Transfer Characteristics

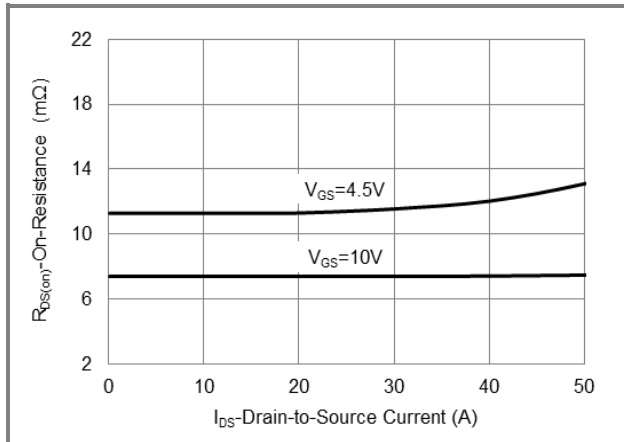


Fig.3 On-Resistance vs. Drain Current

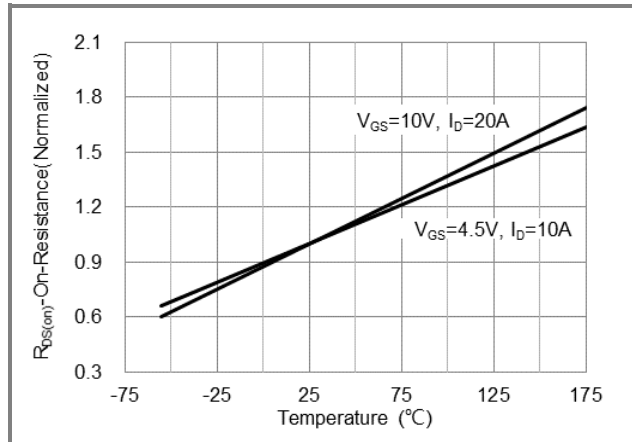


Fig.4 On-Resistance vs. Junction temperature

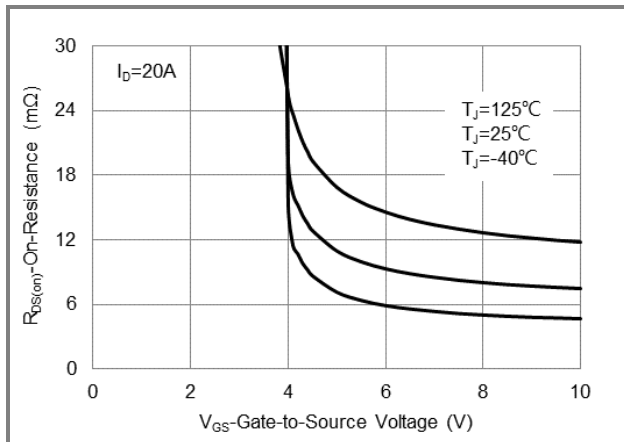


Fig.5 On-Resistance Variation with  $V_{GS}$

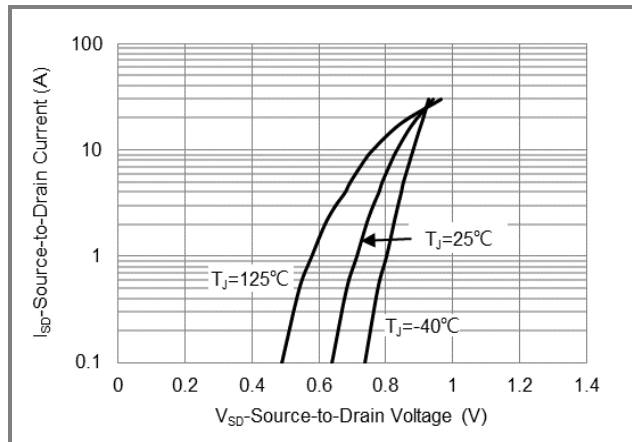


Fig.6 Source-Drain Diode Forward Voltage

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## TYPICAL CHARACTERISTIC CURVES

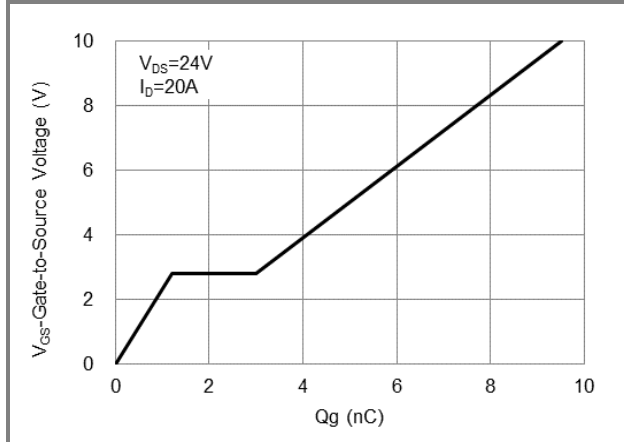


Fig.7 Gate-Charge Characteristics

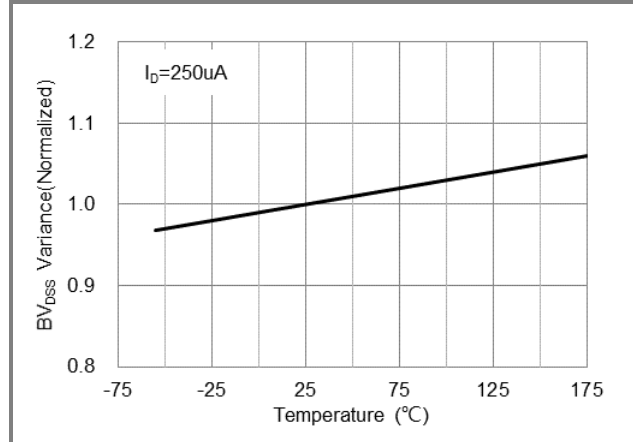


Fig.8 Breakdown Voltage Variation vs. Temperature

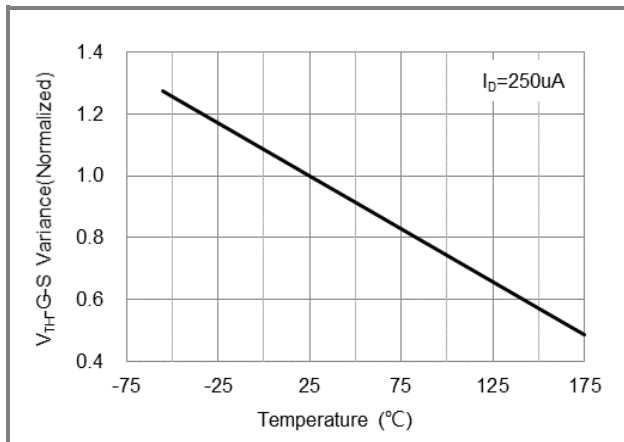


Fig.9 Threshold Voltage Variation with Temperature

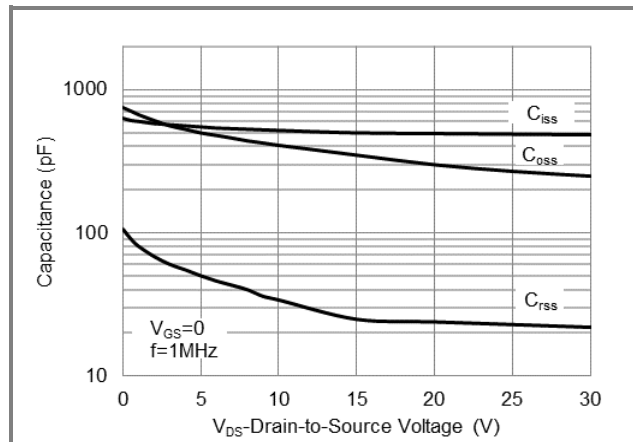


Fig.10 Capacitance vs. Drain-Source Voltage

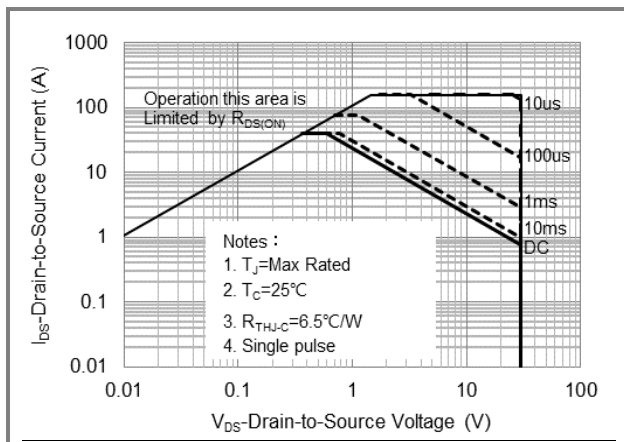


Fig.11 Maximum Safe Operating Area

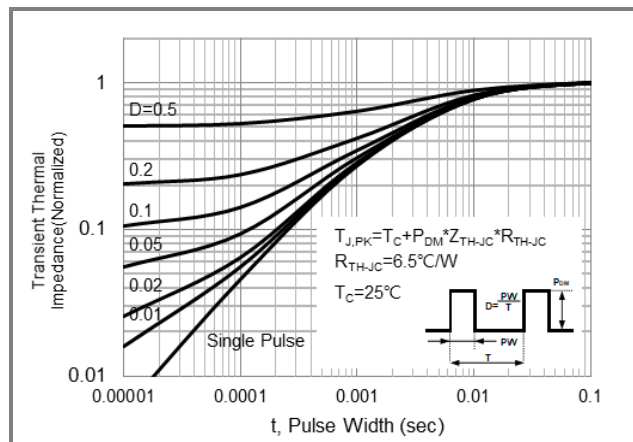


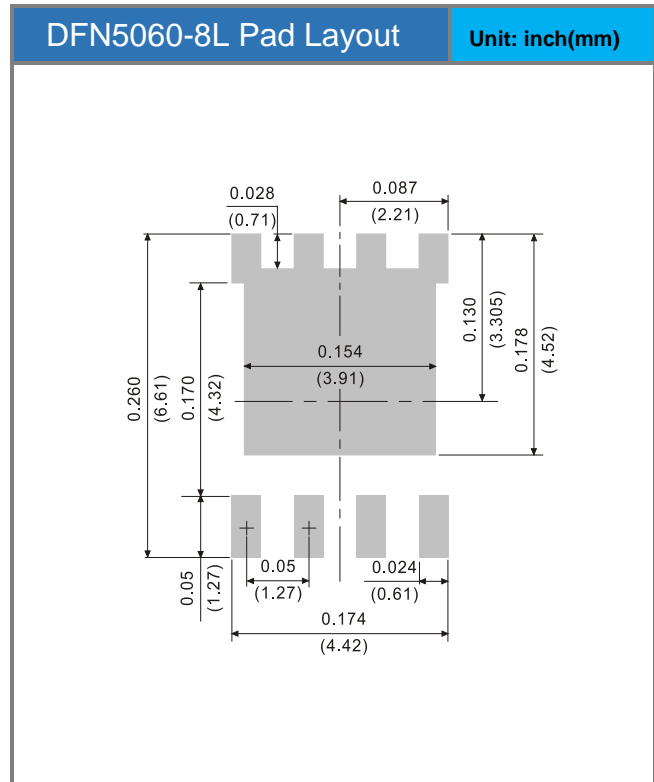
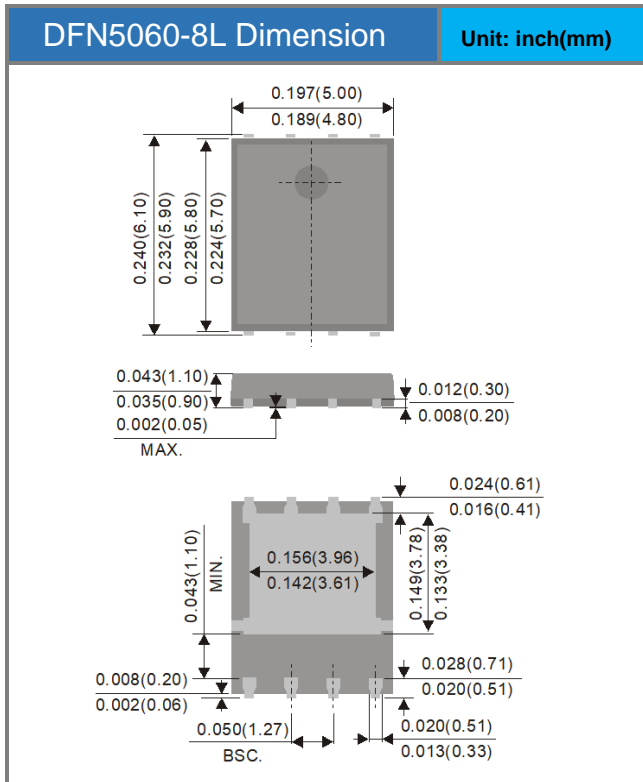
Fig.12 Normalized Transient Thermal Impedance

# PJQ5534-AU

## Product and Packing Information

Part No.	Package Type	Packing Type	Marking
PJQ5534-AU	DFN5060-8L	3K pcs / 13" reel	Q5534

## Packaging Information & Mounting Pad Layout



## PJQ5534-AU

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